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## CSEL INTERFACE UPDATE: K-BAND MICROPROCESSOR DEMONSTRATION

COMPUTER SCIENCES CORPORATION  
6565 ARLINGTON BOULEVARD  
FALLS CHURCH, VIRGINIA 22046

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This technical report has been reviewed and is approved for publication.

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20. ABSTRACT (Continue on reverse side if necessary and identify by block number)  The objective of this demonstration/study is to provide the Air Force with basic data and techniques for expanding the capabilities of the K-Band Terminal Simulator. The current simulator consists of three communication channels, each with several real-time effects (Doppler shift, frequency hop, signal fading, and MFSK) driven by a minicomputer which updates all of these real-time effects every 5 milliseconds. Expansion of the K-Band Terminal Simulator along present lines would increase the		

burden on the minicomputer and therefore increase the basic 5 millisecond time step, which may already be too long for some applications.

The results of this study show that an alternative, vastly superior approach to expansion of the simulator would be to use a separate microprocessor to drive each individual channel. This would relieve the main minicomputer of the fast real-time chores and leave it with only non-time critical system control, operator interface, and housekeeping tasks. This approach would give almost unlimited expansion capability and would allow reducing the basic time step somewhat.

To further assess the feasibility of this approach, a "brassboard" demonstration unit was constructed. This unit uses an 8080 based microprocessor system to drive a frequency synthesizer (the heart of a K-Band Terminal Simulator channel) in real-time from tables of hop, Doppler and MFSK effects. These tables are pre-computed by the CSEL minicomputer from operator input data in a manner similar to that of the existing K-Band Terminal Simulator.

The brassboard demonstration unit ran successfully with an observed time step of 2.45 milliseconds, clearly proving the feasibility of this approach. Complete results, along with all hardware and software documentation are contained in this final report.

A



## PREFACE

This Technical Report was prepared by Computer Sciences Corporation, 6565 Arlington Boulevard, Falls Church, Virginia 22046, for the Air Force Avionics Laboratory under Contract F33615-75-C-1129, job order 12273205. The work on this effort was carried out by Messrs. Douglas O. Alwine, Robert A. Glicksman, Richard G. Murray, and Charles F. Pavey. Lt. Paul F. Humel, USAF, AFAL/AAD, was the project engineer for the Air Force Avionics Laboratory.

## TABLE OF CONTENTS

SECTION I - INTRODUCTION .....	1
SECTION II - DESCRIPTION OF SYSTEM .....	2
SECTION III - RESULTS .....	3
SECTION IV - DESCRIPTION OF HARDWARE .....	6
Control Processor .....	6
Microcomputer .....	6
Frequency Synthesizer .....	9
Opto-Isolator Interface .....	9
Frequency to Voltage Converter .....	9
Connecting Cable .....	9
Power Supply Chassis .....	13
SECTION V - SOFTWARE DESCRIPTION .....	17
Introduction .....	17
Static Mode Module .....	17
Static Mode Mainline .....	20
Block Data .....	30
Subroutine INTELL .....	32
Subroutine COMMO .....	44
Subroutine DL .....	50
Subroutine DOPLD .....	57
Subroutine HOPLD .....	63
Subroutine MFSKLD .....	69
Subroutine ENDSIM .....	75
Subroutine STEPS .....	79
Subroutine IBIE .....	83
Subroutine FREQ .....	88
Subroutine PARMID .....	91
Subroutine SHOW .....	95
Subroutine SEARCH .....	98
Subroutine NUMBER .....	101
Subroutine RLNBCD .....	111
Subroutine RLNASC .....	114
Subroutine RLNBIN .....	117
Subroutine BCD .....	120
Subroutine ASCRLN .....	123
Real-Time Module .....	126

## TABLE OF CONTENTS (Cont'd)

### SECTION V - (CONT'D)

Real-Time Main. ....	127
Reader Program .....	155
Loader Program .....	159



## LIST OF ILLUSTRATIONS

### Figure

1	Block Diagram of the Demonstration System . . . . .	7
2	Opto-Isolator Interface Unit-Schematic Diagram . . . . .	10
3	Frequency to Voltage Converter - Schematic Diagram . . . . .	11
4	Synthesizer Interface . . . . .	12
5	Power Supply Chassis . . . . .	14
6	A. C. Power Control Unit . . . . .	15
7	+8 Volt Power Supply Schematic . . . . .	16
8	System Parameter Table . . . . .	128
9	Pattern Storage Format . . . . .	129
10	Rockland Interface Format . . . . .	131

## SECTION I INTRODUCTION

The objective of this demonstration/study is to provide the Air Force with basic data and techniques for expanding the K-Band Terminal Simulator. The current K-Band Terminal Simulator consists of three signal sources, each capable of a wide variety of modulation types, to simulate a wide variety of transmitters. All three simulated transmitters are driven in real-time by a single minicomputer to simulate the effects of Doppler shift, frequency hop, signal fade, and MFSK modulation. In real life, functions such as Doppler shift and fade are continuous. In order to simulate these functions with a system driven by a digital controller, it is necessary to quantize the changes into discrete steps. In order to have a valid simulation, it is necessary to make these steps very small and hence, they must occur rapidly. The present K-Band Terminal Simulator is capable of outputting updated values for the real-time effects every 5 milliseconds. However, because a single processor is used to drive all of the real-time effects, any expansion of the system, either in the number of carriers or the number of effects per carrier, will necessitate increasing the size of this basic time step.

Since it appears that the Air Force may have the need to increase the number of simulated transmitters and to reduce the basic time step from 5 milliseconds to 1 or 2 milliseconds, it becomes necessary to examine alternative means of controlling the K-Band Simulator. The concept examined here is to control each transmitter simulator in real-time with its own microprocessor, leaving the main minicomputer with only non-time critical system control, operator interface, and housekeeping tasks. This would allow an almost unlimited, modular, expansion capability for the K-Band Terminal Simulator, and expansion could be accomplished without lengthening the time step.

The brassboard demonstration system, described herein, can calculate new values for Doppler shift, frequency hop, and MFSK, add these to the nominal carrier frequency and output an updated frequency to a frequency synthesizer approximately every 2.45 milliseconds.

## SECTION II DESCRIPTION OF SYSTEM

The brassboard demonstration unit consists of a commercial microprocessor development system, programmed to accept standard files from the CSEL minicomputer and drive a frequency synthesizer from these files to simulate Doppler shift, frequency hop, and MFSK. The CSEL PDP-11/20 was programmed to accept operator inputs from the console, build the files, and transfer them to the microprocessor memory.

This demonstration system consists of an INTELLEC 8/MOD 80 microcomputer, a Rockland 5100 frequency synthesizer, and a frequency discriminator to aid in observing the real-time effects on an oscilloscope. Detailed descriptions of this hardware can be found in Section IV.

Values for Doppler shift are taken from the table directly. Values for hop and MFSK are picked pseudorandomly from their respective tables by pseudorandom codes generated in software. These three effects are added to the nominal carrier frequency, converted to the proper format to drive the frequency synthesizer, and outputted, demonstrating clearly the feasibility of controlling the K-Band Terminal Simulator hardware with microprocessors.



### SECTION III RESULTS

The microprocessor was interfaced with the Rockland 5100 frequency synthesizer and the DEC PDP-11/20. It successfully received tables of Doppler shift, hop, and MFSK from the PDP-11/20, and was able to drive the frequency synthesizer in real-time, outputting an updated frequency approximately every 2.45 milliseconds. That is, a new value was calculated for each of the parameters of Doppler shift, MFSK, and frequency hop; that all three new values were added to the nominal carrier frequency and the resulting frequency was formatted and sent to the frequency synthesizer every 2.45 milliseconds. Delay loops were used as necessary to get all output cycles as nearly equal in time as possible. These delay loops would be unnecessary if a real-time clock were incorporated into the microprocessor system. The cost of this clock was not considered justified in this demonstration set-up. Such a clock would be required however, if it is decided to upgrade the K-Band Terminal Simulator with microprocessors, as it would permit the required precise control of the output rate.

The 2.45 millisecond output rate is faster than the present 5 millisecond rate currently available in the K-Band Terminal Simulator, but not nearly as fast as could be attained with some of the newer microprocessors. Many of the newer units offer shorter cycle time and other improvements, such as indirect addressing or an improved instruction set. At least one unit has a 16-bit word length, which could increase speed both by requiring fewer memory cycles to execute a single instruction, (the 8080 fetches as many as three bytes per instruction) and by making it simpler to generate the three 10-bit binary words needed to drive the Rockland synthesizer.

It is not unlikely that a microprocessor could, at this time, be found that would be capable of reducing the observed 2.45 millisecond step time to less than 1 millisecond. New and upgraded microprocessor products are currently being introduced on an almost daily basis and these units offer further improvements in speed, instruction set and I/O flexibility over the original 8080 used in the brassboard demonstration unit. Amid all of this, it is also worthy to note that the prices of microprocessor and related semiconductor products are currently dropping very rapidly. Computer Sciences

Corporation (CSC) feels, therefore, that making a specific recommendation as to the "best" choice of microprocessor at this time would be unjustified. Any information obtained now would soon be too obsolete for the Air Force to use. We, therefore, recommend that the Air Force wait until a microprocessor per access expansion of the CSEL facility is required before attempting to select the "best" microprocessor to use.

A secondary fallout of the rapid drop in semiconductor (specifically memory) prices is a simplification in the recommended configuration for a microprocessor controlled CSEL access. When the processor-per-access technique was first proposed, CSC felt that a practical, operational simulator would have a central core memory which would be maintained by the CSEL minicomputer and shared by each microprocessor controlled access for obtaining hop, Doppler, MFSK, and fade parameters. This configuration required expensive DMA interfaces and attention to critical timing situations. We now feel that the reduced price of semiconductor memory makes it economically feasible for each microprocessor to be provided with enough local RAM memory to store a significant amount of real-time data. The data would be stored in a "double buffer" format, wherein half of the local memory would at any time be filled with current parameters while the other half would be receiving a "downline load" from the CSEL minicomputer. This technique will greatly reduce the complexity of the hardware microprocessor to minicomputer interface and be free of the critical timing burden inherent in a single shared memory system.

The interface between the minicomputer and microprocessor can be either serial or parallel. In the brassboard demonstration system, a 2400 baud serial interface was provided. Approximately 2 minutes was required to transfer the entire set of tables to the microprocessor over this interface. This could be reduced to about 30 seconds by increasing the speed to 9600 baud. For real-time operation on a 1-millisecond time step, and on non-repetitive tables a parallel interface would be required. A serial interface will certainly suffice for repetitive tables, as demonstrated with this brassboard system.

Serial interfaces can be purchased, often complete with software support, at reasonably low cost. Parallel, non-DMA interfaces are generally more expensive and require custom software drivers to be written for them. Parallel DMA interfaces are by far the most expensive in both hardware and software and generally produce the greatest number of integration problems. Therefore, the particular operational requirements of a microprocessor-per-access simulator will have to be considered when attempting to configure such a system in the most cost-effective manner.



## SECTION IV DESCRIPTION OF HARDWARE

The hardware block diagram is shown in Figure 1. The major blocks of this diagram are described below.

### CONTROL PROCESSOR

The PDP-11/20 is the processor that is normally used to drive the K-Band Terminal Simulator. The software prepared for the PDP-11 (see Section 5) allows the operator to build tables of values for frequency hop, MFSK, and Doppler, and transfer these tables to the microcomputer memory. The interface to the PDP-11 is through a DL11 interface module normally used to drive a second VTO5 console.

### MICROCOMPUTER

The microcomputer in the block diagram is an INTELLEC 8/MOD 80 development system. While a number of microprocessor chips were available at the start of the contract, only the Intel 8080 was available off-the-shelf, with the support hardware and software needed to develop this system.

The microcomputer supplied for this demonstration has the following modules:

- 1 - IMM8-83 CPU Module
- 2 - IMM8-61 I/O Cards
- 1 - IMM8-63 Output Card
- 2 - IMM6-28 Random Access Memory Cards, 4K each
- 3 - IMM6-26 PROM Cards, 4K bytes each
- 1 - IMM6-76 PROM Programmer
- 1 - Front Panel Control Module

The microcomputer is normally supplied with one IMM8-61 I/O card and a second was added to provide a serial interface to the DEC DL11-C I/O module. An IMM8-63 output card was added to provide output ports to drive the synthesizer.

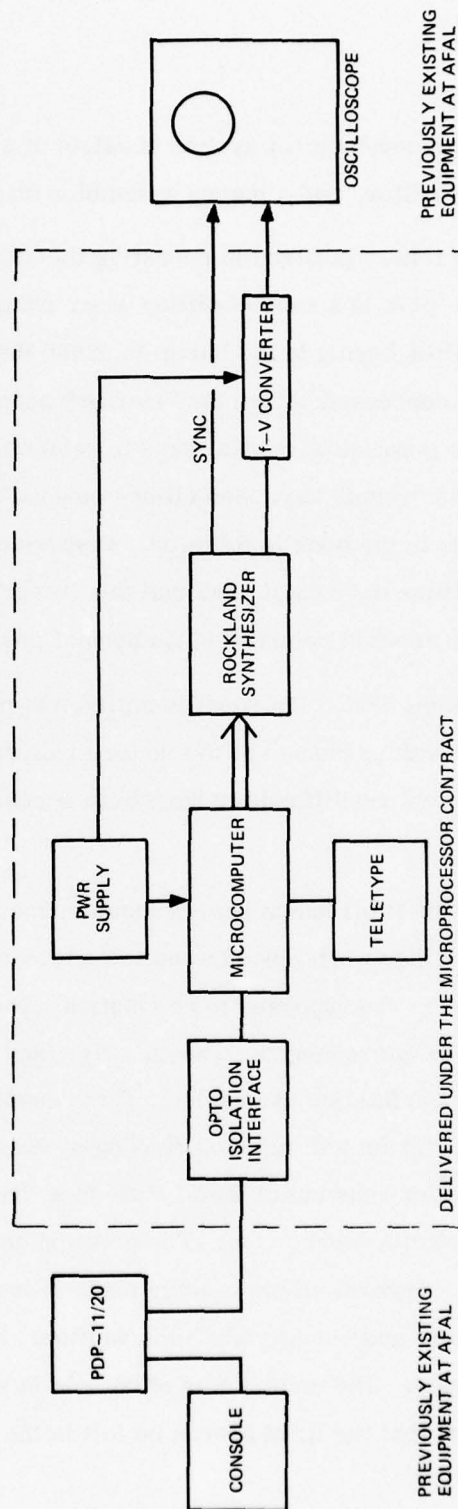


Figure 1. Block Diagram of the Demonstration System

The software included with the development system consists of a system monitor that resides in 2K of PROM, a text editor, and a macro assembler on paper tape.

CSC has found several peculiarities involved in operating this device that the Air Force should be cognizant of. The first is a race condition when bringing up the System Monitor which can be avoided if, after keying in the "jump to 3800" instruction in locations 0, 1, and 2, the reset key is depressed before the "memory access" key is returned to its normal position. The instruction manual says to return the "mem access" key to normal before depressing the "reset" key. Sometimes several tries are required to start the machine if the sequence in the book is followed. Discussions with the factory have verified that a race condition does exist, and that the "reset" key should be depressed first, then the "memory access" returned to its normal position.

The second peculiarity is simply that if the room is chilly, the machine needs a few minutes to warm up. Discussions with personnel at the factory indicate that this is normal. After 5-10 minutes of operation, no difficulties have been encountered, even when the room was quite cool.

The third peculiarity is that the two random access memory modules must be installed in the same slots in which they were placed when the microprocessor was delivered to AFAL. The two modules are supposed to be identical, and indeed they will usually function normally if they are interchanged. The only time any memory problem has been apparent is when running the Intellec assembler. If the assembler is run with the memory cards reversed, the program will not stop reading at the end of the source tape, but will continue until the reader runs out of tape. This is a "hard" error, occurring every time an attempt is made to read a source tape. The problem goes away when the two RAM boards are interchanged. Several attempts were made to isolate the error by writing various patterns into memory and reading what was written. No error was ever found, and the attempt was abandoned. The factory was of no help in explaining this situation, other than recommending that the RAM boards be left in the position wherein no problems were encountered.



## FREQUENCY SYNTHESIZER

The frequency synthesizer is a Rockland model 5100. This unit was chosen for its fast switching speed and its ability to switch frequency without any phase discontinuity in the output. A synthesizer with these features was required in order to obtain small Doppler steps at a fast rate.

A description of this device can be found in the manufacturer's manual.

## OPTO-ISOLATOR INTERFACE

Both the DEC DL11 and the Intel IMM8-61 I/O modules utilize a serial, current-loop output, and were designed to drive a console such as a CRT or a teletype. These modules were interfaced with opto-isolators (see Figure 2). An opto-isolator consists of a light emitting diode (LED) and a phototransistor, mounted in a common package. Forward current through the LED causes it to emit light which turns on the transistor. This arrangement provides a high degree of electrical isolation, avoiding the problems with ground loops that might occur if the grounds of the two machines were connected together.

## FREQUENCY TO VOLTAGE CONVERTER

The frequency-to-voltage converter was constructed as an aid in determining if the output of the frequency synthesizer is being varied correctly. A schematic diagram of this assembly is shown in Figure 3. The CA3012 limiter amp provides a constant level to the input of the monostable flip flop (74121). A pulse train is produced at the one shot output with all pulses being the same width, but with a pulse repetition rate equal to the frequency of the synthesizer output.  $R_2$  and  $C_2$  average the output of the one shot. Since the pulse width is constant, the dc voltage across  $C_2$  is proportional to the frequency. Hence, the output voltage is proportional to the synthesizer output frequency.

## CONNECTING CABLE

The values outputted to the synthesizer are transmitted via an IMM8-63 output module. A list of the wiring, from the rear panel of the microcomputer to the synthesizer input is shown in Figure 4. An additional, individual wire coming from the

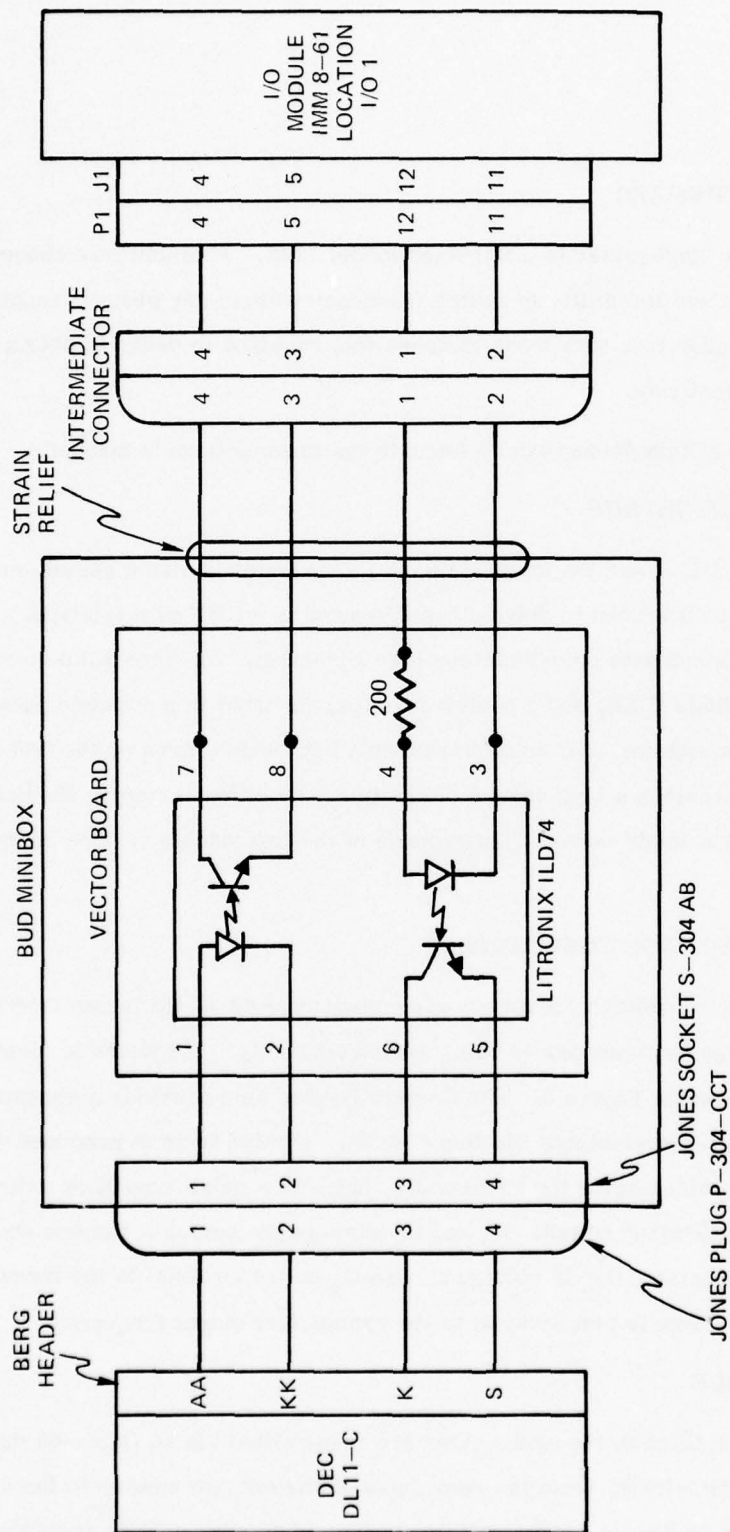


Figure 2. Opto-Isolator Interface Unit - Schematic Diagram

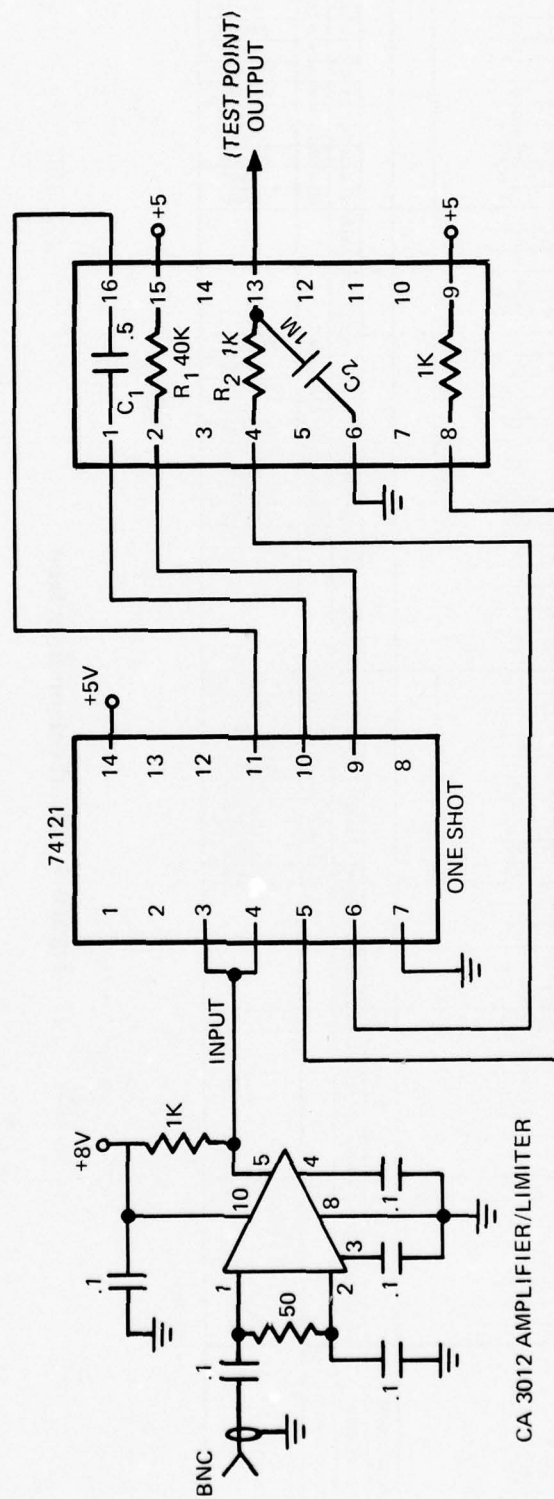


Figure 3. Frequency to Voltage Converter - Schematic Diagram





synthesizer connector carries a software generated load pulse, pin 12, which is used for troubleshooting, for synchronizing an oscilloscope, or for measuring the rate at which the synthesizer frequency is being updated on a counter.

#### POWER SUPPLY CHASSIS

This chassis contains six assemblies, A1 through A6 (see Figure 5). The functions of these assemblies are as follows.

Connector J48 on the rear of the Intellec is an AC connection for a teletype. An AC card from assembly A1 is plugged into this outlet (see schematic, Figure 6). When the microcomputer is turned on, it energizes relay K1, which energizes the teletype and the three power supplies, A4, A5, and A6. A6 is a -10 volt supply and A5 is a +5 volt supply. These two supplies are needed to supplement the ones inside the Intellec when the microprocessor system consists of more than a CPU, 2 RAM boards, 1 ROM board, and 2 I/O boards. If the output board driving the synthesizer is removed, and the extra ROM board in ROM slot 2 is removed, the internal power supplies are sufficient, and the external ones can be removed. The external power supplies are adequate to power the computer with all card slots filled.

Assemblies A2 and A3 are the opto-isolator interface and the frequency to voltage converter, respectively. Both units have already been discussed.

A4 is a +8 volt power supply which is used to power the CA3012 limiter/amplifier in the frequency to voltage converter. A schematic diagram of this unit is shown in Figure 7.

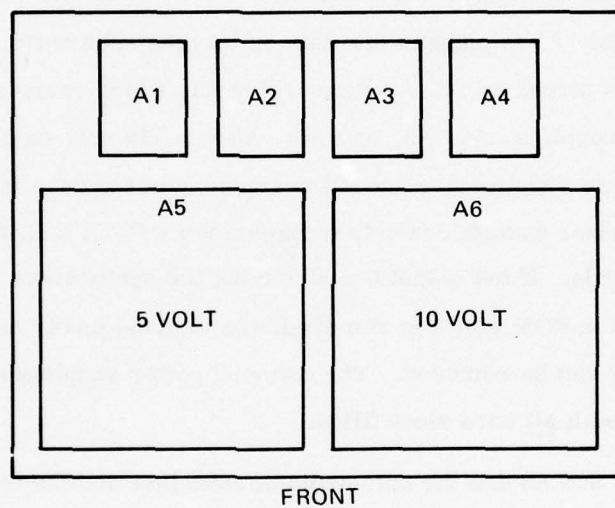


Figure 5. Power Supply Chassis



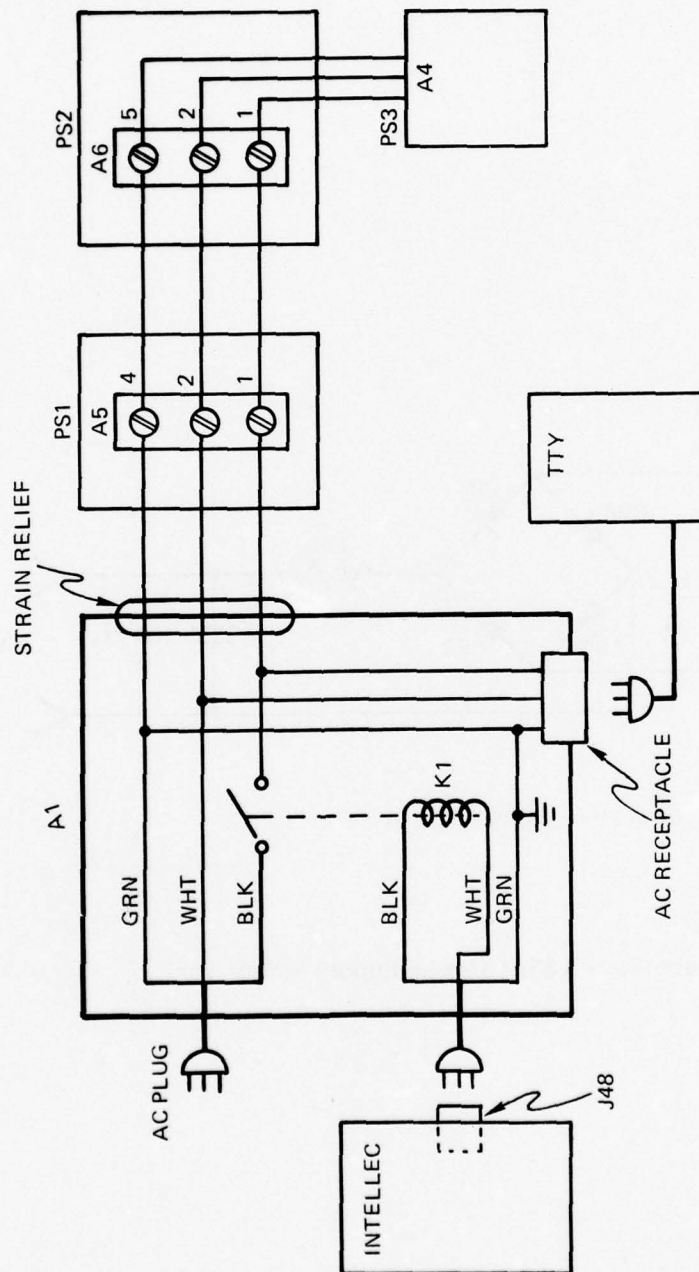
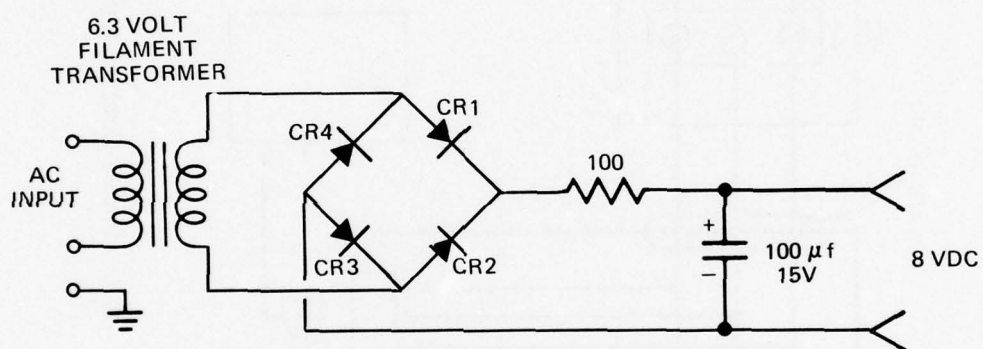


Figure 6. A.C. Power Control Unit



CR1-CR4 = IN599

Figure 7. +8 Volt Power Supply Schematic

## SECTION V SOFTWARE DESCRIPTION

### INTRODUCTION

The software for the brassboard demonstration system is comprised of two modules — a static mode module and a real-time module. The static mode module is responsible for building and transmitting the system parameter tables and pattern value tables to the Intellec microprocessor. The real-time module is responsible for the execution of the real-time mode.

Detailed documentation on each main program and subroutine in the demonstration software system follows. This documentation includes a description of each module, program, and subroutine, a flowchart, and a computer listing.

### STATIC MODE MODULE

The static mode module is responsible for building and transmitting the system parameter and pattern value tables used in the real-time mode. This module is comprised of a mainline program and many functional subroutines.

All variable elements in the system parameter table are input via the system console using keywords to specify a particular variable. Each keyword has an associated subroutine that is responsible for managing the input of its associated parameter value. A listing of the keywords and associated subroutines appears in Table 1.

Prior to conversion to real-time form, each effect parameter value established through console input is stored in labeled common as a four byte BCD value. During conversion to real-time form, each BCD value is converted to double precision and then to the binary form of the real-time mode. This process could have been simplified using the DECODE system routine, but would have defeated our design objective of attempting to keep the module as system independent as possible.

HOP and MFSK table values are input by the module through the console. The table size for each must be a power of two with a maximum size of 64 for MFSK and 128 for HOP. The Doppler values are built by successive additions of an operator supplied



offset to the base frequency. The MFSK and HOP values are converted to BCD form and then to their packed decimal storage form. The DOP offset is also converted to BCD form, but is then converted to double precision for the addition process used in determining each successive value. Each value so generated must be converted from double precision to packed decimal. Subroutines internal to the module are used for the conversions from BCD to double precision and from double precision to packed decimal.

Transmission of system parameter and table values is performed via the subroutines designed to transfer data according to an expected sequencing of the real-time mode reader program. Error checking is performed in these subroutines to guarantee the successful transfer of the data to the Intellec microprocessor. An assembly language routine is used to perform the actual byte transfers to the Intellec using the DL11 interface. This is the only system and machine dependent element of the module.

Besides the transmission error checking, the module also performs extensive error checking of operator input for illegal input strings and values out of range. A final consistency check is also performed on the value tables to ensure that only valid frequencies will be output in real-time mode by the frequency synthesizer. Error messages are output to the system console if errors are detected.

Labeled common errors are used extensively throughout the module for communication between the subroutines in the module. All areas are initialized in a BLOCK DATA subprogram. A description of each area, purpose, and initial values is contained in the BLOCK DATA subprogram description.

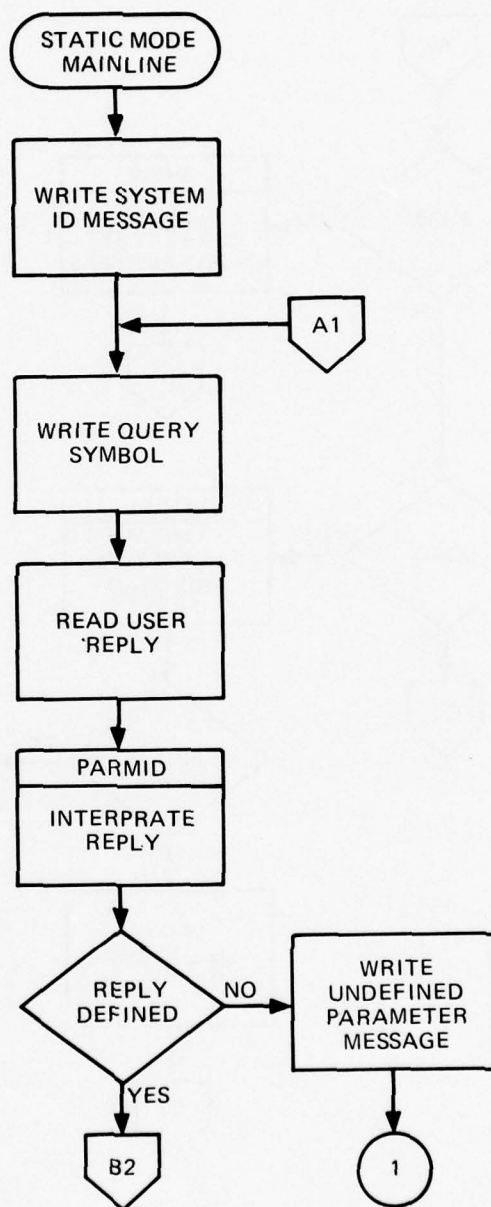
TABLE 1. SYSTEM KEYWORDS

<u>KEYWORD</u>	<u>DESCRIPTION</u>	<u>SUBROUTINE</u>
SHOW	Display current values of effect start, end, cycle, base frequency, and simulation end.	SHOW
LOAD	Perform system parameter and pattern value transfer	INTELL
FREQ	Input base frequency value	FREQ
HOPL	Input HOP table values	HOPLD
MFSL	Input MFSK table values	MFSKLD
DOPL	Build DOP table	DOPLD
HSTR	Input HOP start time	IBIE
MSTR	Input MFSK start time	IBIE
DSTR	Input DOP start time	IBIE
HEND	Input HOP end time	IBIE
MEND	Input MFSK end time	IBIE
DEND	Input DOP end time	IBIE
HCYC	Input HOP cycle value	STEPS
MCYC	Input MFSK cycle value	STEPS
DCYC	Input DOP cycle value	STEPS
SEND	Input simulation end value	ENDSIM

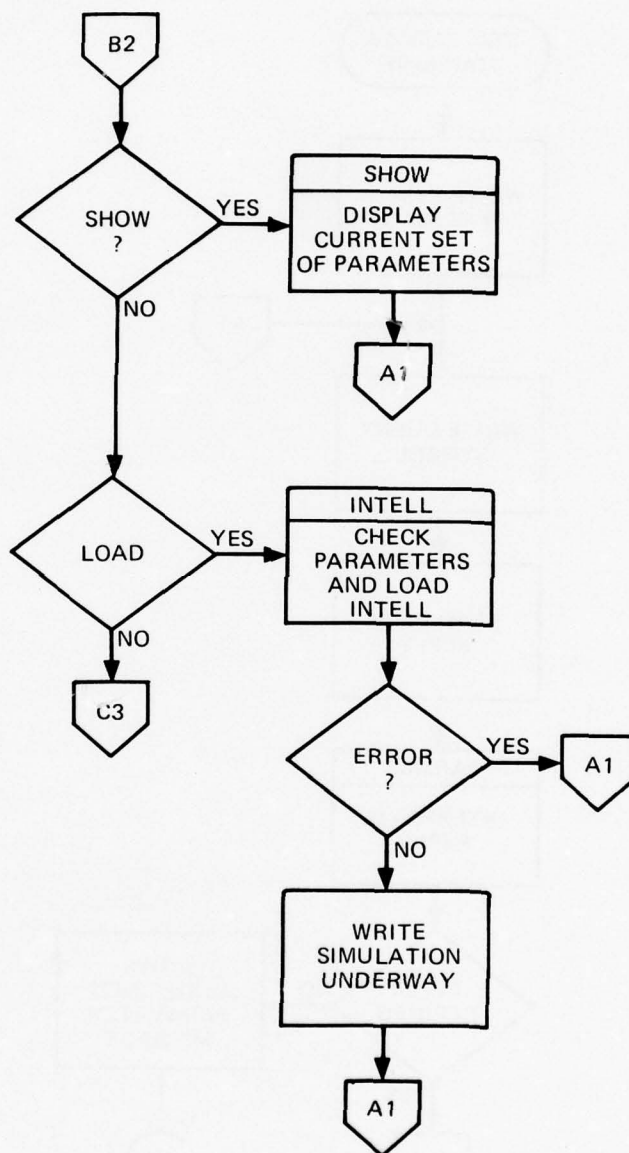
## STATIC MODE MAINLINE

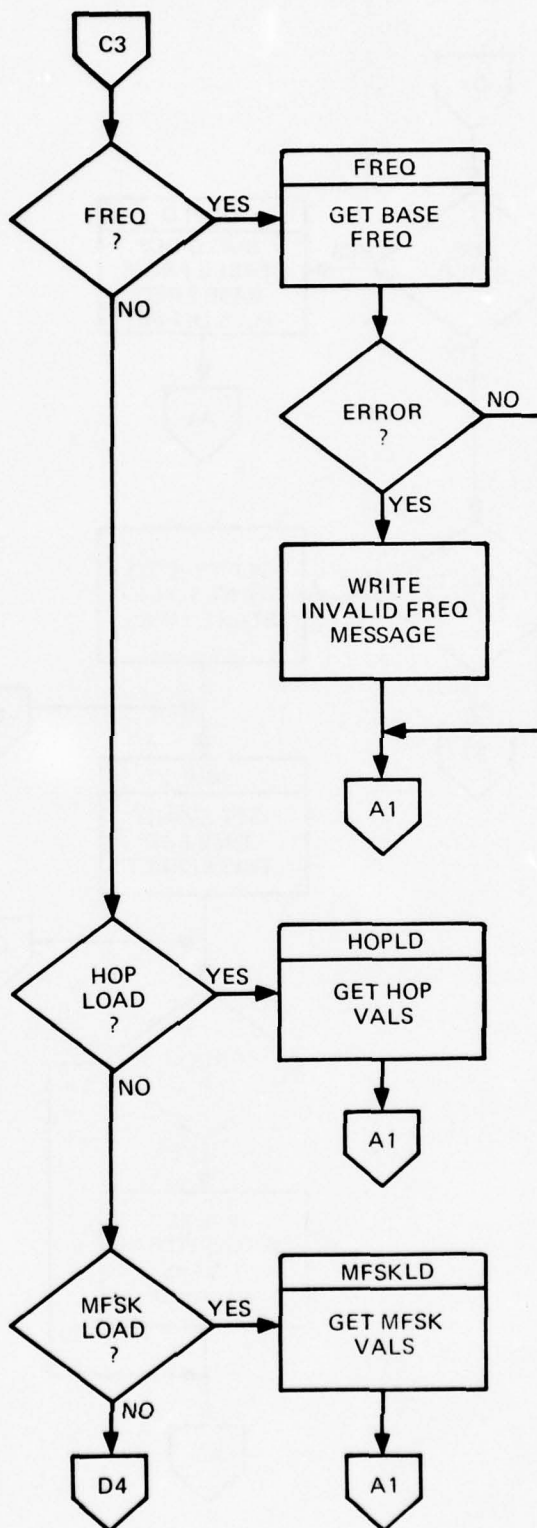
This program is used to perform input of the function keywords that govern system setup and execution and to call the appropriate subroutine that manages the execution of the keyword specified.

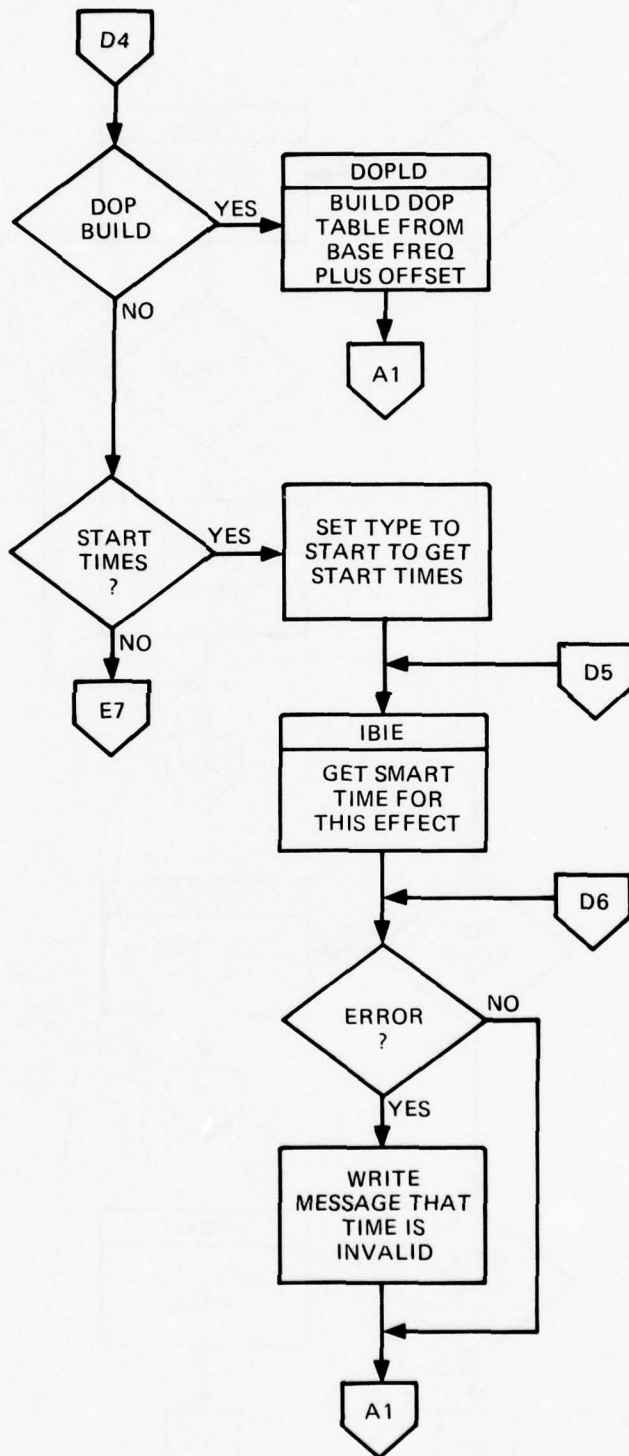
The "PARMID" routine is used to determine the identity of the function keyword supplied. This program successively examines the value returned from the routine to determine the appropriate subroutine to invoke to complete the keyword processing.

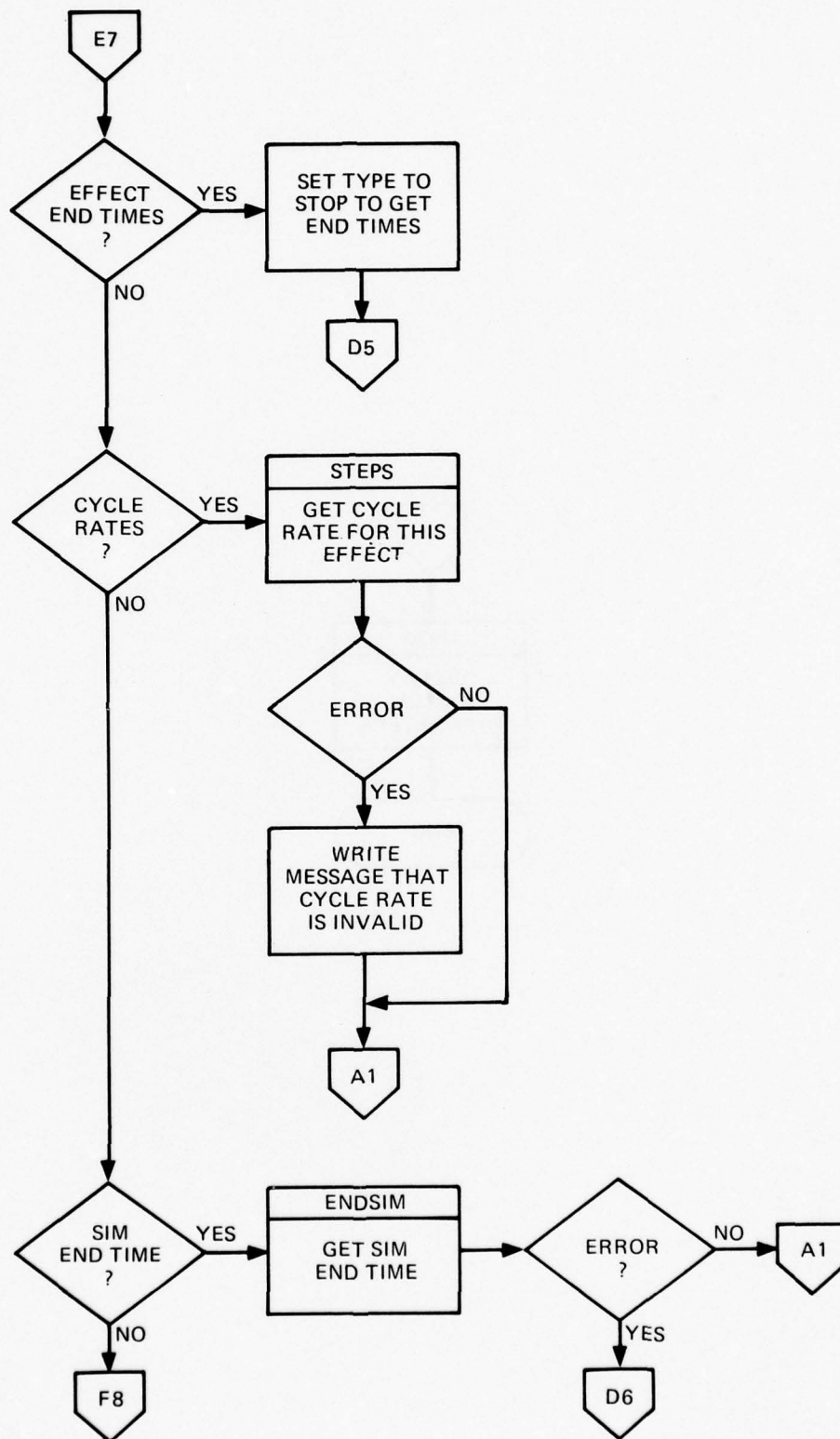




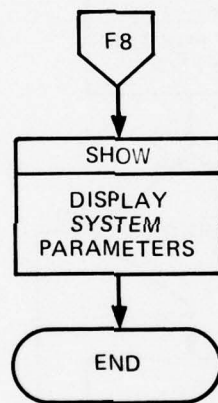












```

C*****
C
C KBRAND DEMONSTRATION STATIC MODE PROGRAM
C
C**** THIS IS THE MAINLINE PROGRAM FOR THE KBRAND MICROPROCESSOR
C**** DEMONSTRATION SYSTEM. ITS MAIN FUNCTION IS TO QUERY THE
C**** USER FOR A FUNCTION KEYWORD AND CALL THE APPROPRIATE
C**** ROUTINE THAT WILL PERFORM THAT FUNCTION. THE PARAMIO
C**** THAT IDENTIFIES THE FUNCTION TO BE PERFORMED. THE KEYWORDS
C**** AND INDICES ARE AS FOLLOWS.
C SHQ=1 LOAD=2 FREQ=3 HOP=4 MFSL=5
C DUPL=6 HSTR=7 MSTR=8 USTR=9 MEND=10
C MEND=11 MEND=12 MCYC=13 MCYC=14 UCYC=15
C SEND=16
C
C*****
C COMMON/SYSTEM/START,STOP,PCYCLE,PBASE,PSMEND,MASK
C COMMON/TABLES/HOP,POP,MFSK
C COMMON/INLINE/INLINE
C COMMON/SPDEC/CHARS,ICAR
C BYTE CHARS(25)
C BYTE INLINE(24),HOP(640),POP(5120),MFSK(320),PBASE(12)
C REAL PCYCLE(3)
C REAL PSTAT(3),PSTOF(3),PSMEND,TYPE,R
C INTEGER MASK(3)
C**** WRITE SYSTEM IDENTIFICATION MESSAGE
C**** WRITE(6,910)
900 FORMAT(1H,'*****KBRAND MICROPROCESSOR DEMO SYSTEM*')
C**** WRITE QUERY SYMBOL
910 WRITE(6,911)
901 FORMAT(1H,'S',/)
C**** READ USER REPLY INTO INLINE
C**** READ(6,922)INLINE
902 FORMAT(24A1)
C**** INTERPRATE REPLY-RETURN NUMERIC IDENTIFIER
C**** CALL PARPID(INLINE)
C**** IF(INLINE.GT.0)GO TO 20
C**** WRITE(6,924)
904 FORMAT(1H,'***UNDEFINED PARAMETER*')
C**** GO TO 10
20 IF(INLINE.GT.1)GO TO 40
C**** DISPLAY CURRENT SET OF SYSTEM PARAMETERS
C**** CALL SHOW
C**** GO TO 10
40 IF(INLINE.GT.2)GO TO 60
C**** CHECK SYSTEM PARAMETERS,LOAD INTELL,AND GO
C**** CALL INTELL(IERR)
C**** IF(IERR.GT.0)GO TO 10
C**** WRITE(6,920)
920 FORMAT(1H,'***SIMULATION UNDERWAY*')
C**** GO TO 100
60 IF(INLINE.GT.3)GO TO 80
C**** GET BASE FREQUENCY FROM USER
C**** CALL FREQ(IERR)
C**** IF(IERR.EQ.0)GO TO 10

```

```

      WRITE(6,9.16)
      FORMAT(1H , '***INVALID FREQUENCY')
      GO TO 10
      IF (IND.GT.4) GO TO 100
      C**** BUILD MOP TABLE FROM USER FREQS
      CALL MOPL
      GO TO 10
      IF (IND.GT.5) GO TO 120
      C**** BUILD MFS TABLE FROM USER FREQS
      CALL MFSKLD
      GO TO 10
      IF (IND.GT.6) GO TO 140
      C**** GENERATE JOPPLER TABLE FROM BASE AND USER OFFSET
      CALL JOPL
      GO TO 10
      IF (IND.GT.9) GO TO 160
      C**** GET EFFECT START TIMES IN MINUTES FROM USER
      TYPE='STAR'
      CONTINUE
      CALL LDE(IND,TYPE,IERR)
      IF (IERR.NE.0) GO TO 10
      WRITE(6,9.28)
      IF (IND.GT.12) GO TO 180
      C**** GET EFFECT END TIMES IN MINS FROM USER
      TYPE='STOP'
      GO TO 150
      IF (IND.GT.15) GO TO 200
      C**** GET EFFECT CYCLE RATES FROM USER IN #CYCLES
      CALL STEPS(IND,IERR)
      IF (IERR.GT.0) WRITE(6,9.10)
      IF (IERR.GT.0) GO TO 10
      IF (IERR.GT.0) GO TO 155
      C**** DISPLAY SYSTEM PARAMETERS BEFORE EXITING
      1000 CALL SHOW
      END

```

```

ROUTINES CALLED:
PARMID, SHOW , INTELL, FREQ , MOPLO , MFSKLD, JOPLD
101E , STEPS , ENDSIM
OPTIONS #/ON,/SU,/OP:1

```

```

BLOCK      LENGTH
MAIN.      489      (001722)*
SYSTEM     29      (000072)
TABLES     3040     (013700)
INBUF      10      (000024)
SPCODEC    11      (000026)

```

FURTRAN V06.13

00106106

21-JAN-76

PAGE

3

\*\*COMPILER ----- CORE\*\*  
PHASE USED FREE  
DECLARATIVES 01027 02139  
EXECUTABLES 01023 01943  
ASSEMBLY 01485 06121



## BLOCK DATA

The purpose of this subprogram is to initialize the labeled common areas of the static mode module prior to its execution. A listing and description of each area follows:

1. RTMTB - a 31 word integer array that initializes the system parameter table used in the real-time mode. The real-time pattern masks, random number seeds, and pattern table addresses are non zero.
2. MAXMIN - a 6 element double precision array used to store the HOP, MFSK, and DOP maximum and minimum values.
3. TABLES - a 6080 byte area used for pattern value storage in packed decimal form. This area is initialized to zero.
4. SYSTEM - a 29 word integer area used for the BCD intermediate storage of effect start, stop, cycle values, base frequency value, and simulation end. This area is initialized to zero.
5. SPCDEC - a 22 byte area used to store the ASCII character representations for those characters used in operator input processing.



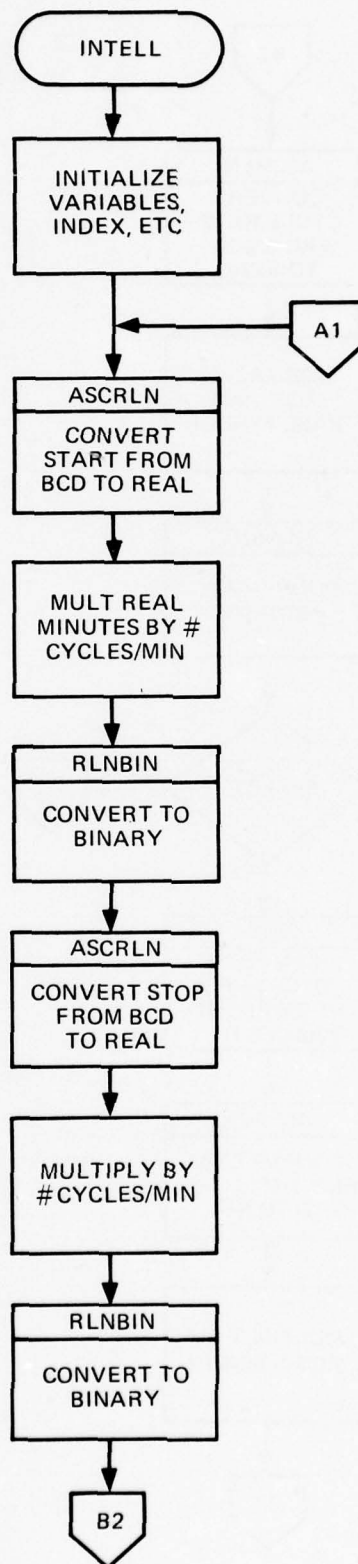
#### SUBROUTINE INTELL

The primary purpose of this routine is to manage the conversion and transmission of the system parameter values and pattern value tables to the Intellec microprocessor. This routine also checks the consistency of the pattern value tables to ensure that a frequency less than 0 or greater than 2 megahertz cannot be generated.

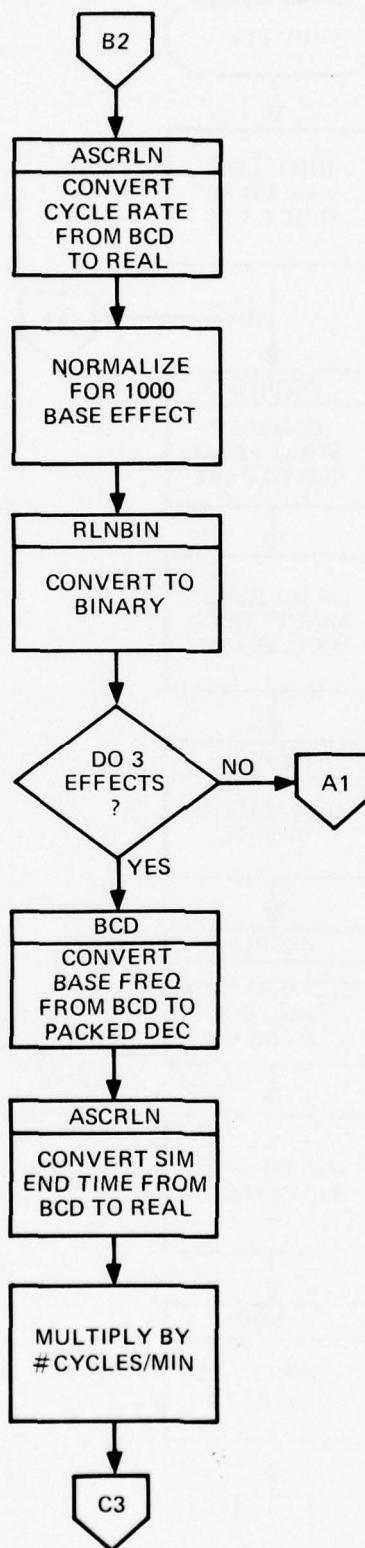
The simulation end and the three effect start, stop and cycle values are first converted from BCD to real number values using the ASCRLN subroutine. Simulation end and effect start/stop values which are specified in minutes are then converted to number of cycles per minute. The values are then converted to the binary form of the real-time mode with the RLNBIN subroutine.

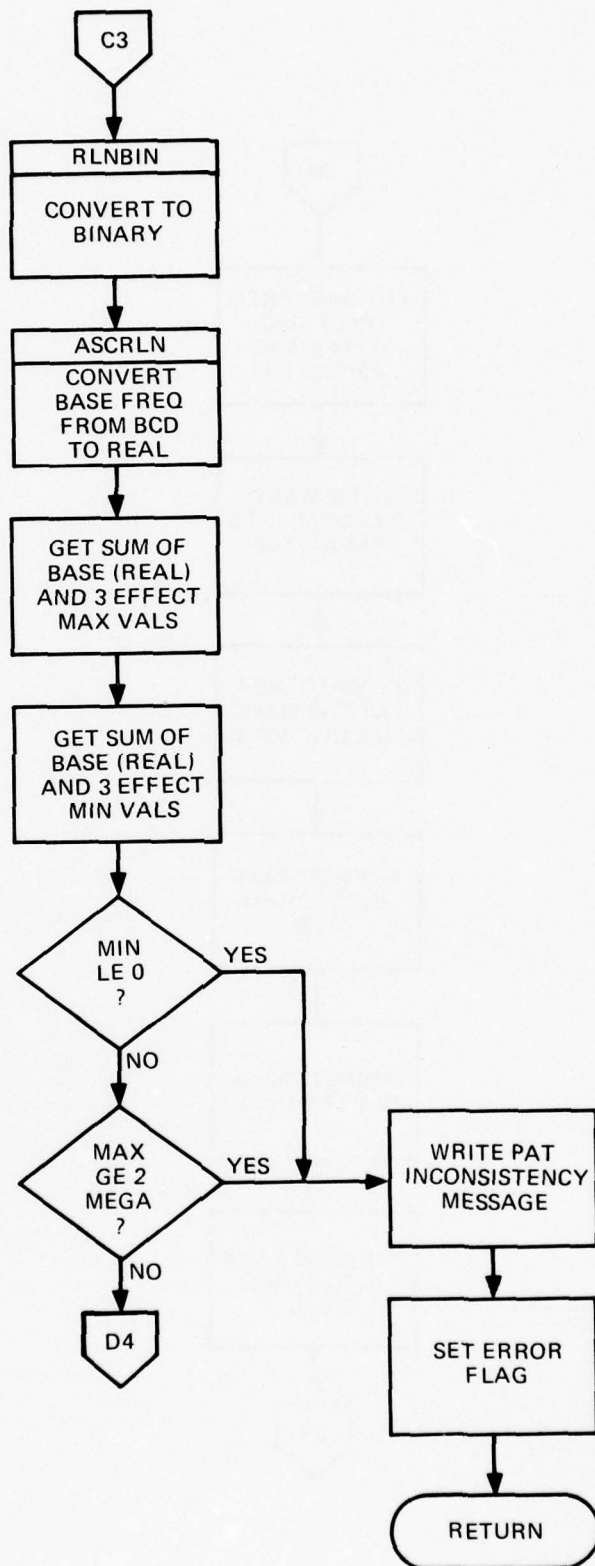
After conversion, the simulation end, effect start, stop, cycle values, and base frequency value in packed decimal form are inserted into the "TAB" array. The "TAB" array is a 61 byte table that is initialized in BLOCK DATA with the system parameter elements that are constant; i. e., pattern mask, running sum, addresses etc. Data transmission to the Intellec is done in the following order using the COMMO subroutine:

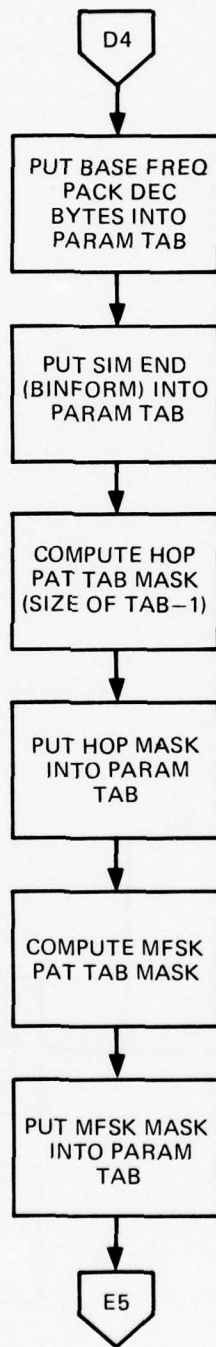
1. System parameter table - 61 bytes starting at location 20 HEX.
2. HOP pattern value table - 640 bytes transmitted in 32 byte blocks beginning at location 1A00HEX.
3. MFSK pattern value table - 320 bytes transmitted in 32 byte blocks beginning at location 1D00HEX.
4. DOP pattern value table - 5120 bytes transmitted in 32 byte blocks beginning at location 600 HEX.

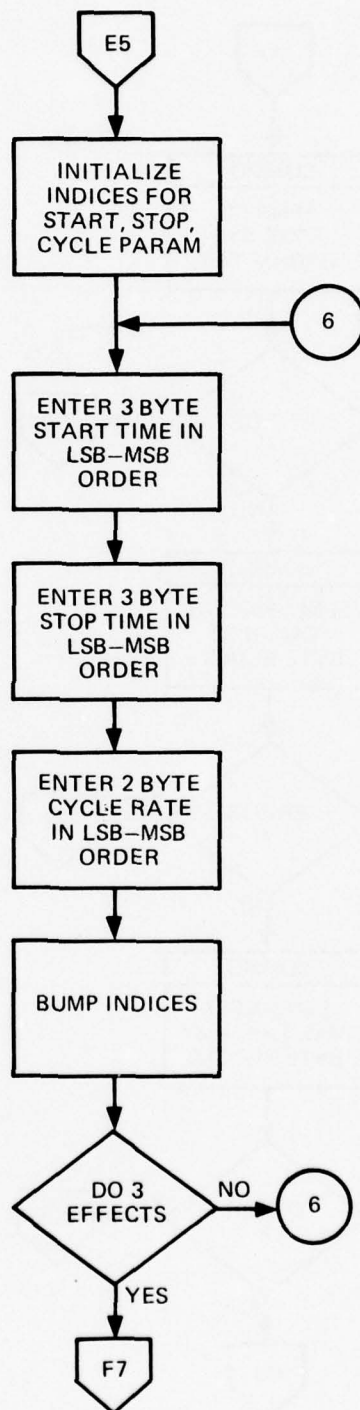




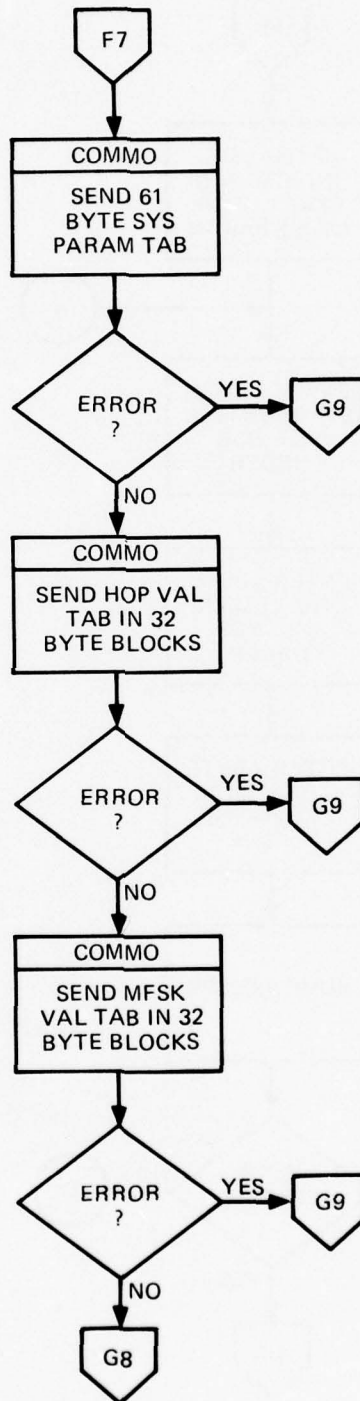


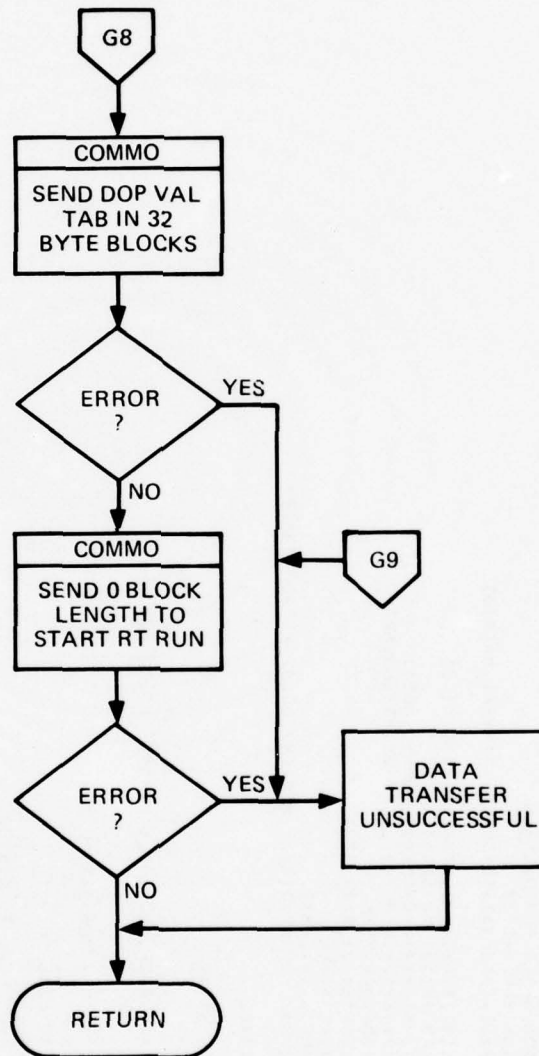












```

C***** SUBROUTINE INTELL(IENR)*****
C
C***** THE PURPOSE OF THIS ROUTINE IS TO CONVERT THE REAL TIME
C***** PARAMETERS INTO THE BINARY INTELL FORM, CHECK THE CONSISTENCY
C***** OF THE PATTERN TABLES, AND TO LOAD THE INTELL.
C
C*****
C***** INTEGER S/SADR, MOPADR, MFSADR, DOPADR, ADR
C***** BYTE DAT(32)
C***** COMMON/RT/TAB/TAH
C***** COMMON/MAXMIN/RMAX, RMIN
C***** DOUBLE PRECISION MMAX(3), RMIN(3)
C***** DOUBLE PRECISION SFREQ, HFREQ, LFREQ
C***** DOUBLE PRECISION RLN, FACTOR
C***** INTEGER ISTART(6), ISTOP(6), ICYCLE(6), IEND(2), MASK(3)
C***** BYTE TAB(6*2)
C***** INTEGER ISENO(4), ISTART(12), ISTOP(12), CYCLE(12)
C***** BYTE IVAL(12), PHASE(12), IVASE(5)
C***** REAL PSTART(3), PSTOP(3), PCYCLE(3), PSMEND, ASCII
C***** COMMON/SYSTEM/PISTART, PSTOP, PCYCLE, PHASE, PSMEND, MASK
C***** COMMON/TABLES/MOP, DOP, MFSK
C***** BYTE MOP(144), DOP(512), MFSK(320)
C***** DOUBLE PRECISION SCALE
C***** EQUIVALENCE (ASCII, IVAL(S))
C***** DATA SYSADR/2002A7, MOPADR/21A00/, MFSADR/21D00/, DOPADR/20600/
C***** SCALE=26606.
C***** FACTOR=SCALE/1000.
C***** DO 5 I=1,12
C***** ZLRO BCD STRING ARRAY
C***** IVAL(I)=
C***** 5 CONTINUE
C***** CONVERT THE START, STOP, AND CYCLE PARAMETERS TO BIN
C***** J=1
C***** DO 10 I=1,3
C***** PUT START INFO INTO BYTES 5-8 OF IVAL
C***** ASCII=PISTART(I)
C***** CONVERT START TO REAL
C***** CALL ASCHN(IVAL, RLN)
C***** CONVERT START FROM REAL TO BINARY
C***** RLN=FACTOR*RLN
C***** CALL RLNIN(RLN, ISTART(J))
C***** PUT STOP INFO INTO BYTES 5-8 OF IVAL
C***** ASCII=PSTOP(I)
C***** CONVERT STOP TO REAL NUMBER
C***** CALL ASCHN(IVAL, RLN)
C***** CONVERT STOP FROM REAL TO BINARY
C***** RLN=FACTOR*RLN
C***** CALL RLNIN(RLN, ISTOP(J))
C***** PUT CYCLE INFO INTO BYTES 5-8 OF IVAL
C***** ASCII=PCYCLE(I)
C***** CONVERT CYCLE RATE FROM BCD TO REAL
C***** CALL ASCHN(IVAL, RLN)
C***** CONVERT CYCLE FROM REAL TO BINARY
C***** RLN=RLN/100.

```

```

C===== CALL RLNIN(RLN,CYCLE(J))
C===== J=J+4
C===== CONTINUE
C===== CONVERT BASE FREQ FROM HCD STRING TO INTELL FIRM
C===== CALL HCD(BASE,IFASE)
C===== PUT SIM END TIME INTO BYTES 5-8 OF IVAL
C===== ASCII2P5END
C===== CONVERT SIM STOP TIME TO REAL NUMBER
C===== CALL ASCIIN(IVAL,RLN)
C===== CONVERT IT TO BINARY
C===== RLN=ACTVAL*RLN
C===== CALL RLNIN(RLN,SIMEND)
C===== CONVERT BASE FREQ TO RLN FOR PATTERN LIMIT CHECK
C===== CALL ASCIIN(PHASE,SPREQ)
C===== HPREQ=SPREQ
C===== CHECK IF A PATTERN CAN BE GENERATED IN INTELL THAT IS
C===== OUT OF LIMITS(A=20000000000)
C===== DO 50 I=1,3
C===== HPREQ=HPREQ+HMAX(I)
C===== HPREQ=HPREQ+HMIN(I)
C===== CONTINUE
C===== 50
C===== IF (HPREQ*.1)GO TO 800
C===== IF (HPREQ*.2)GO TO 800
C===== BUILD TABLE TO BE SENT TO INTELL
C===== DO 20 I=1,5
C===== BASE FREQUENCY
C===== TAB(I+1)=IBASE(I)
C===== CONTINUE
C===== 20
C===== DO SIMULATION END
C===== DO 30 I=2,4
C===== TAB(I8-I)=SIMEND(I)
C===== CONTINUE
C===== DETERMINE MASK VALUES FOR RAN NUMB GENERATOR
C===== K=MASK(I)=1
C===== TAB(20)=K+1
C===== K=MASK(2)=1
C===== TAB(35)=K+1
C===== POINTN TO SET OF 3 START BYTES PER EFFECT
C===== J=J7
C===== POINTN TO SET OF 3 STOP BYTES PER EFFECT
C===== K=K9
C===== POINTN TO SET OF TWO CYCLE BYTES PER EFFECT
C===== L=L27
C===== ENTER EFFECT START, STOP, AND CYCLE VALUES INTO SYS ARRAY
C===== DO 40 I=1,9,4
C===== EFFECT START TIMES
C===== TAB(J)=START(I+3)
C===== TAB(J+1)=START(I+2)
C===== TAB(J+2)=START(I+1)
C===== EFFECT END TIMES
C===== TAB(K)=STOP(I+3)
C===== TAB(K+1)=STOP(I+2)
C===== TAB(K+2)=STOP(I+1)
C===== EFFECT CYCLE MATRS

```



```

TAB(L)=CYCLE(I+3)
TAB(L+1)=CYCLE(I+2)
C==== BUMP TO NEXT EFFECT START,STOP,CYCLE VALUE INPUT
J=J+15
L=K+15
L=L+15
40 CONTINUE
C==== NOW USE SUB COMMO TO SEND DATA TO INTELL
C==== FIRST SEND SYSTEM PARAMETER TABLE
CALL COMMO(SYSADR,61,TAB,IERR)
IF (IERR.GT.0) GO TO 650
C==== NOW SEND HOP TABLE
ADR=HOPADR
C==== GET ADR OF LOCATION FOR 32 BYTE BLOCK
DO 120 I=1,5089,32
C==== LOAD UP 32 BYTE BLOCK
DO 110 J=1,32
DAT(J)=HOP(I+J-1)
110 CONTINUE
C==== SEND BLOCK OF 32 BYTES
CALL COMMO(ADR,32,DAT,IERR)
IF (IERR.GT.0) GO TO 650
C==== BUMP TO NEXT BLOCK ADR
ADR=ADR+32
120 CONTINUE
C==== SEND MFSK TABLE TO INTELL
ADR=MFSKADR
DO 140 I=1,289,32
C==== LOAD UP 32 BYTE BLOCK
DO 130 J=1,32
DAT(J)=MFSK(I+J-1)
130 CONTINUE
C==== SEND BLOCK OF 32 MFSK BYTES TO INTELL
CALL COMMO(ADR,32,DAT,IERR)
IF (IERR.GT.0) GO TO 650
C==== BUMP TO NEXT MFSK TABLE ADDRESS
ADR=ADR+32
140 CONTINUE
C==== SEND DOPELER TABLE TO INTELL
ADR=DOPELADR
DO 160 I=1,5089,32
C==== LOAD UP 32 BYTE BLOCK
DO 150 J=1,32
DAT(J)=DOPEL(I+J-1)
150 CONTINUE
C==== SEND BLOCK OF 32 BYTES
CALL COMMO(ADR,32,DAT,IERR)
IF (IERR.GT.0) GO TO 650
C==== BUMP TO NEXT DOP ADR IN INTELL
ADR=ADR+32
160 CONTINUE
C==== SEND 0 BYTE COUNT TO SIGNIFY LOADING COMPLETE
CALL COMMO(ADR,0,DAT(1),IERR)
IF (IERR.EQ.0) RETURN
C==== MSG GENERATED NOT IN 0-2 MEGA RANGE
650 WRITE(6,1-20)IERR

```

FUTRAN V06.13

00:07:00 21-JAN-76 PAGE 4

1020 FORMAT(1H,'DATA TRANSFER TO INTELL NOT SUCCESSFUL-ERROR=',IS)

RETURN

900 CONTINUE

800 WRITE(6,02)

802 FORMAT(1H,'PATTERN TABLE INCONSISTENCY')

10001

RETURN

END

ROUTINES CALLED:

ASCMLN, RLNBIN, BCD , COMMO

OPTIONS =/ON,/SU,/OP:1

BLCK LENGTH

INTELL 854 (003254)\*

HTMTAB 31 (000076)

MAXMIN 24 (000060)

SYSTEM 29 (000072)

TABLES 3040 (013700)

\*\*COMPILER ----- CORE\*\*

PHASE USED FREE

DECLARATIVES 00022 02344

EXECUTABLES 01347 01569

ASSEMBLY 01721 05085

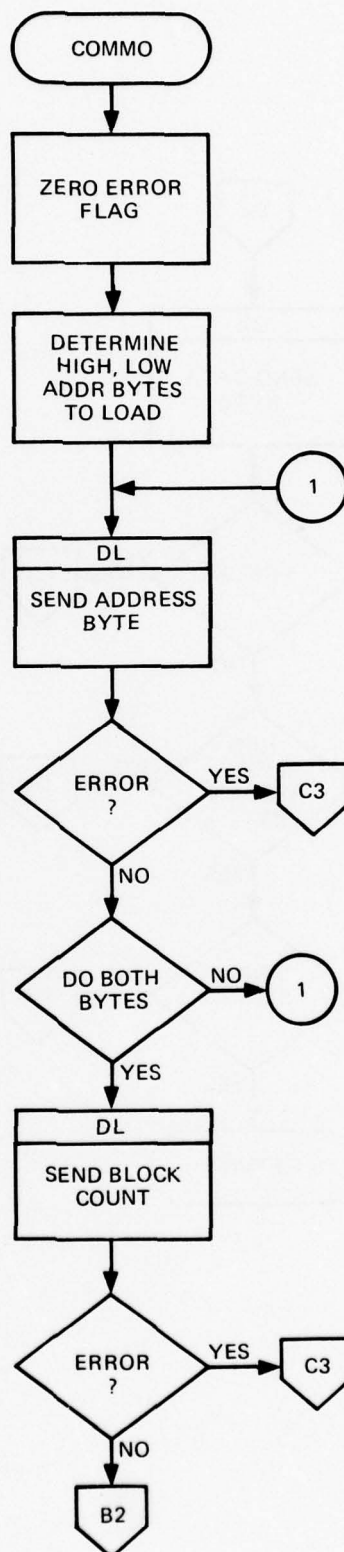
#### SUBROUTINE COMMO

The purpose of this routine is to transmit a block of data via the DL11 interface and the DL subroutine to the Intellec microprocessor.

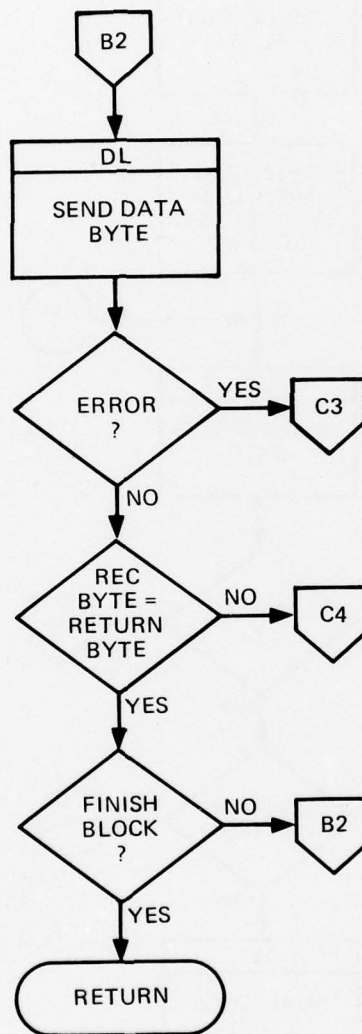
The address of the memory location to load, the number of bytes in the block, and the data block are passed to the routine. The routine then passes this information via the DL subroutine to the Intellec in the following order.

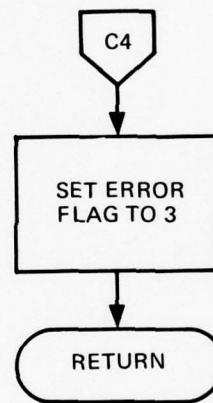
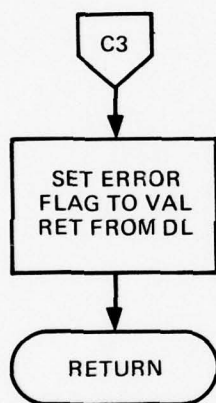
1. High byte address.
2. Low byte address.
3. Number of bytes in the data block.
4. The data bytes one at a time.

After each transfer, the error flag returned from the DL subroutine is checked for possible errors. If an error occurs, the routine returns the value of the DL subroutines error flag to the caller. The byte passed to the DL subroutine is also compared with the byte echoed back from the Intellec after each byte transfer to verify correct reception. An error value of three is returned from this routine if a verification error occurs.









[illegible]

FORTRAN V06.13

00:07:57

21-JAN-70

PAGE

2

COMMO 215 (000656)\*

\*\*COMPILER ----- CORE\*\*  
PHASE USED FREE  
DECLARATIVES 00622 02344  
EXECUTABLES 00783 02183  
ASSEMBLY 01081 06525

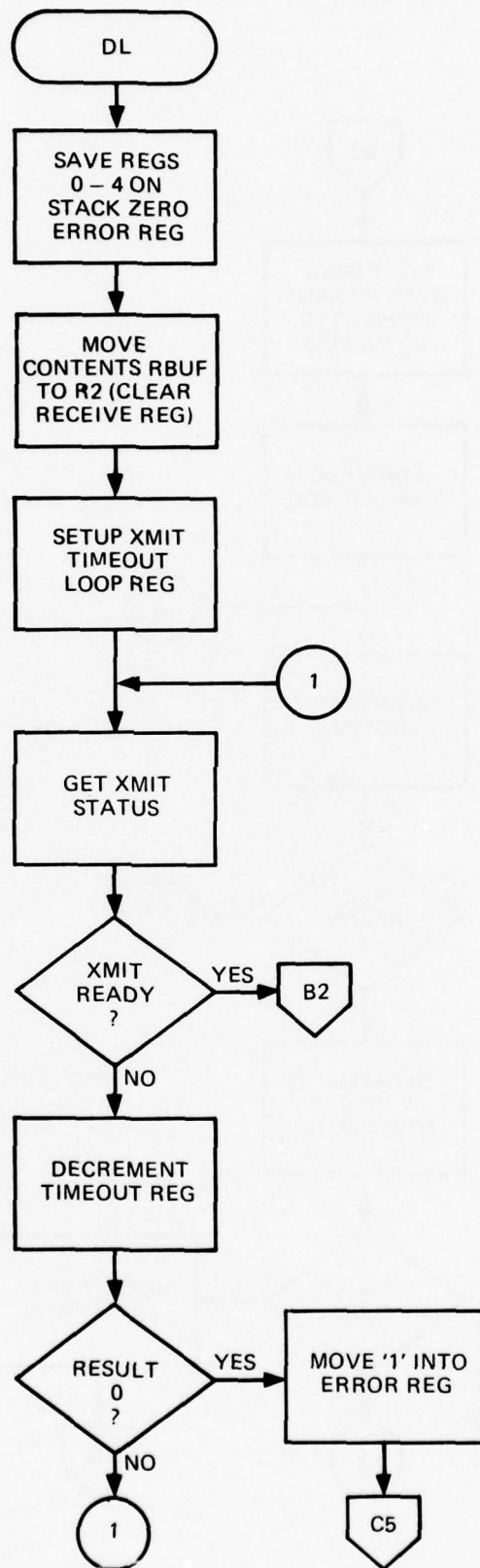


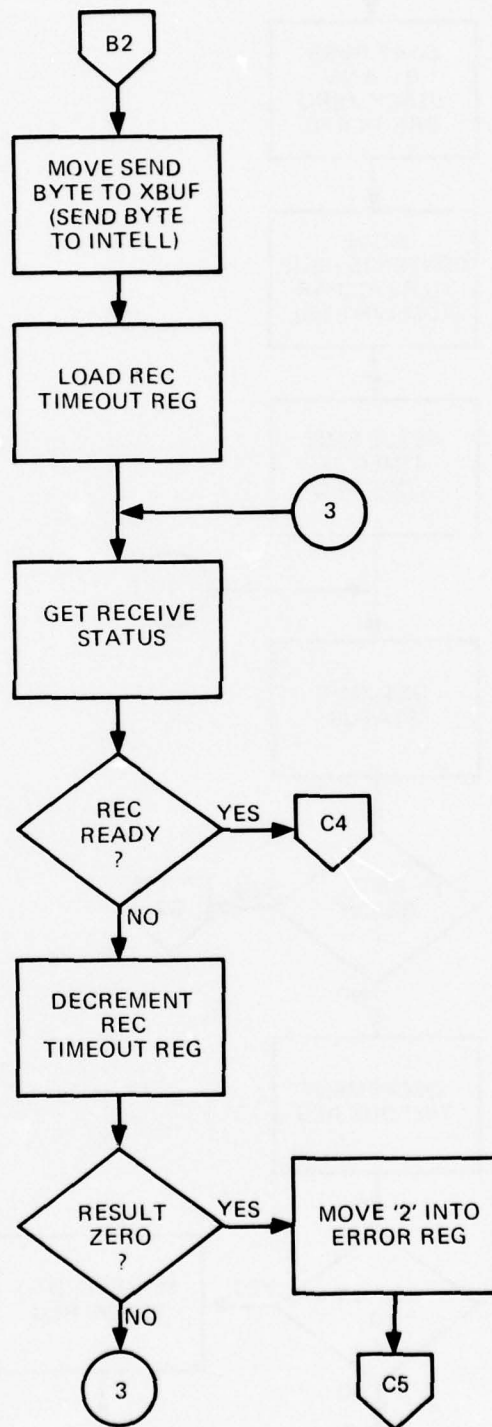
#### SUBROUTINE DL

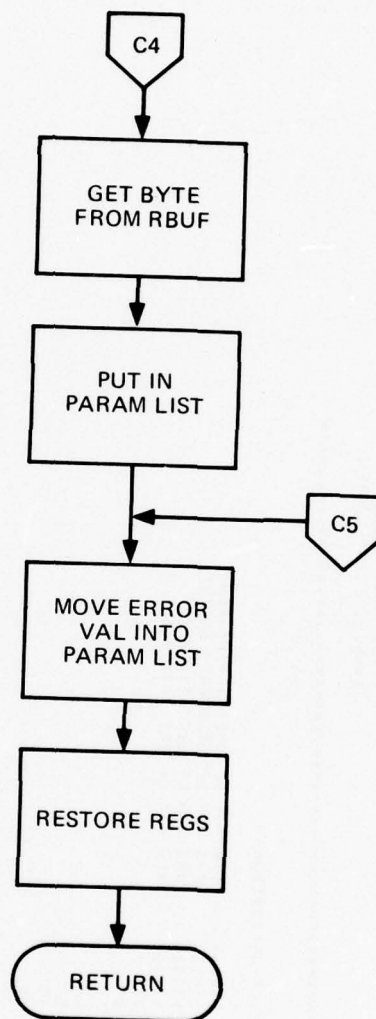
This routine is used to transmit and receive byte data to and from the Inteltec via the DL11 interface. A byte to be transmitted is passed to the routine in its parameter list. After transmission of the byte to the Inteltec, the routine loops checking the receive status for indication that the byte sent has been echoed back. Once the receive indicator in RCSR becomes true, the echoed byte is moved from RBUF to the callers argument list.

The routine also returns an error flag to the caller that is set as follows:

1. 0 = no errors
2. 1 = XMIT ready not received
3. 2 = REC ready not received











```

DL
55 00220 013702 XSTAT: MOV      @XCSR,R2 JGET XMIT STATUS
56 00232 232702 BIT          #200,R2 JTEST BIT 7 FOR XMIT READY
57 00236 001000 BNE          XMIT      JBIT 7=0, THEN OK TO SEND
58 00240 005301 DEC          R1
59 00242 001371 BNE          XSTAT J TRY AGAIN TO GET XMIT OK
60 00244 212703 MOV          #1,R3 J XMIT NOT READY ERROR
61 00250 000167 JMP          REST
62
63 J**** SEND THE BYTE TO THE INTELL
64
65 00050 117537 XMIT: MOV      #2(R5),@XBUF
66
67 J**** GET BYTE RECEIVED INDICATION
68
69 00062 012701 MOV      #7777,R1 J ECHO TIMEOUT REG
70 00066 013702 RSTAT: MOV      @XCSR,R2 JGET REC STATUS
71 00072 232702 BIT          #200,R2 JTEST BIT 7 FOR REC READY
72 00076 001000 BNE          REC      J BIT 7=0, THEN GOT BYTE BACK
73 00080 005301 DEC          R1
74 00082 001371 BNE          RSTAT J AGAIN CHECK FOR BYTE FROM INTELL
75 00084 212703 MOV          #2,R3 JREC TIMEOUT
76 00086 000167 JMP          REST
77
78 J**** GET BYTE ECHOED FROM INTELL
79 00090 013702 REC: MOV      @XBUF,R2 JSIGN EXTEND THE RECEIVED BYTE
80 00094 012703 MOV          R2 ,@4(R5) JPUT WORD IN PARAMETER LIST
81
82 J**** SET COMPLETION FLAG AND RESTORE REGS
83
84 00124 010375 RSTAT: MOV      R3,@6(R5)
85
86 00130 012600 MOV      (SP)+,R0
87 00132 012601 MOV      (SP)+,R1
88 00134 012602 MOV      (SP)+,R2
89 00136 012603 MOV      (SP)+,R3
90 00138 012604 MOV      (SP)+,R4
91 00140 000205 RTS          R5 J RETURN TO CALLER
92
93 .END

```

DL  
SYMBOL TABLE

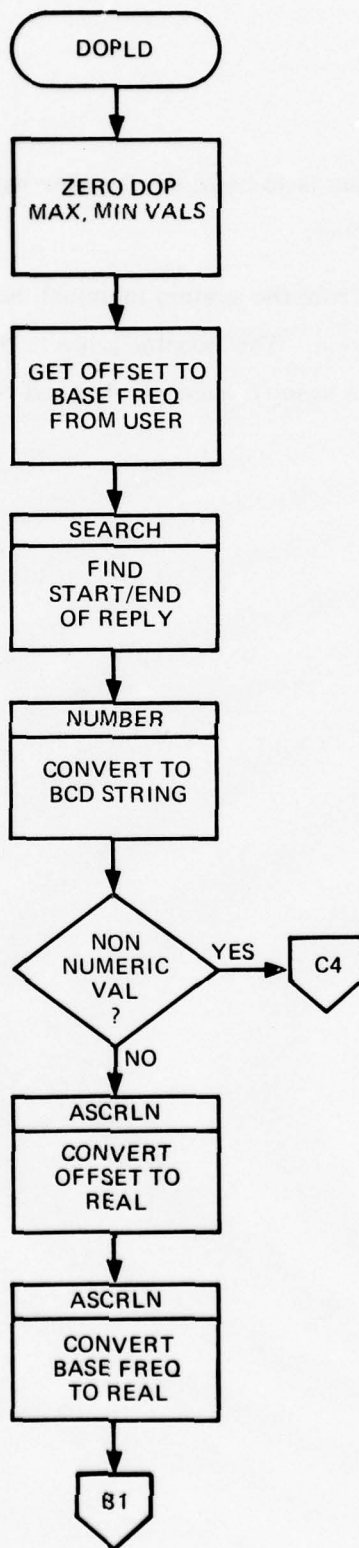
DL	00000000	RBUF	= 176512	RCSR	= 176510
REC	000114H	REST	= 000124R	RSTAT	= 000066R
XBUF	= 176516	XCSR	= 176514	XMIT	= 000054R
XSTAT	000026R				
* ADS	000000				
	000				
	00144				
ERRORS DETECTED:	0				
FREE CORE:	4523				
PART4,OBJ,LPI<PART4,MAC					

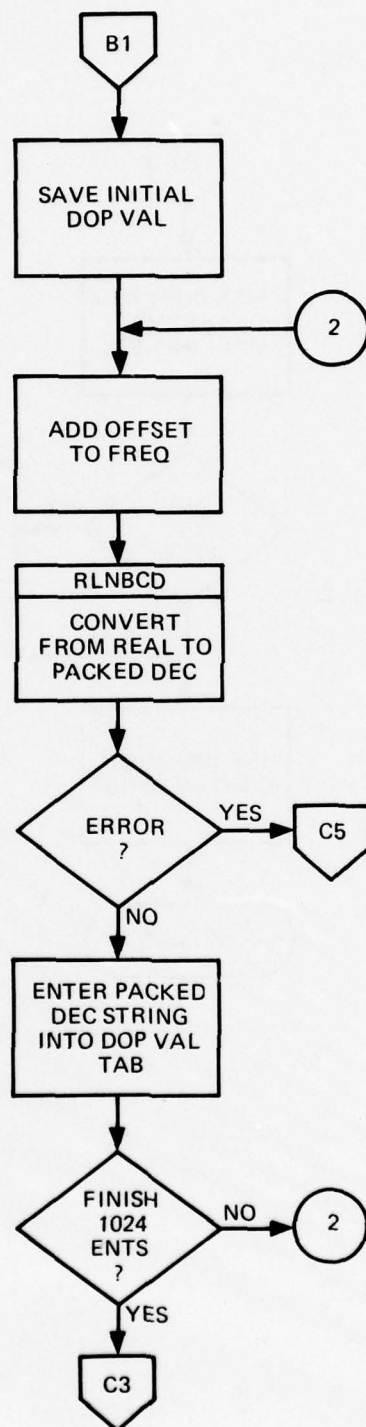
#### SUBROUTINE DOPLD

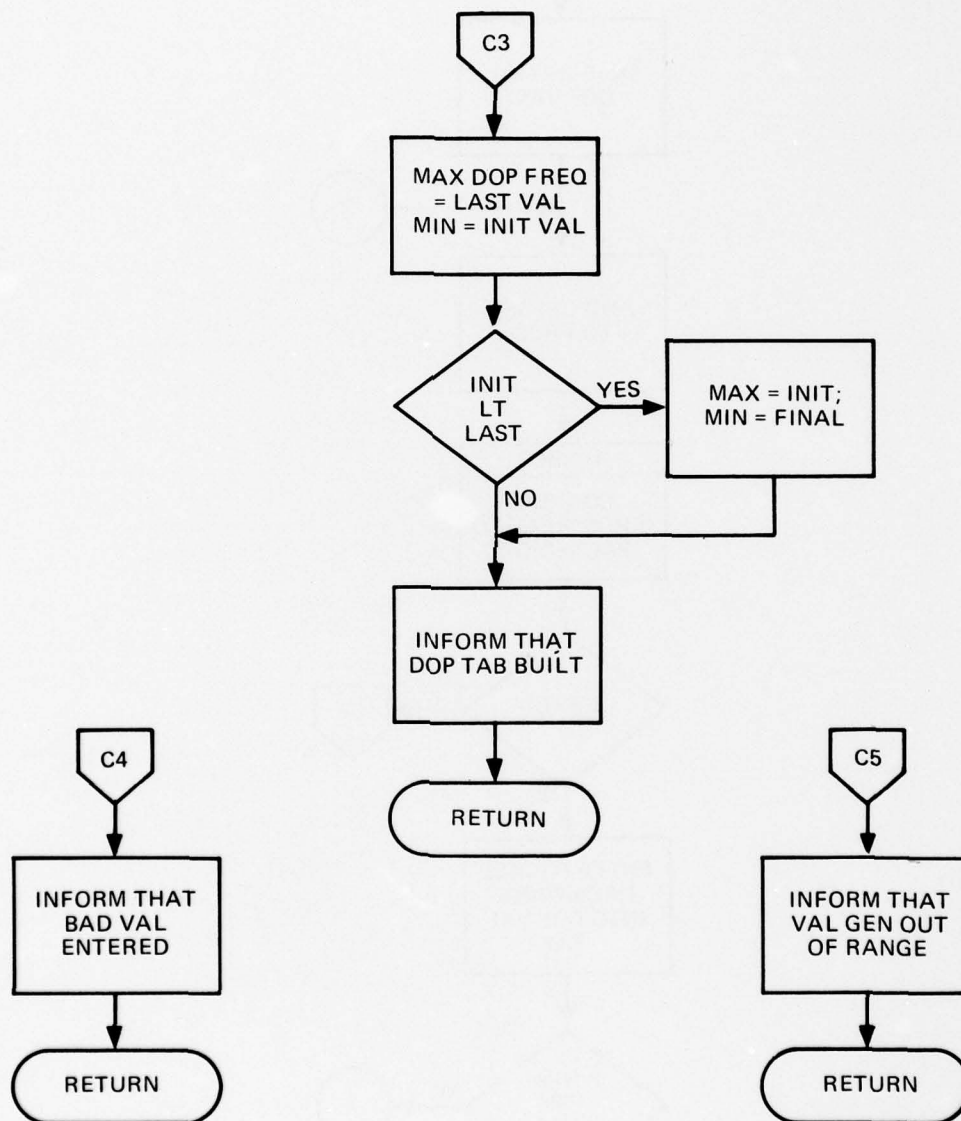
The purpose of this routine is to build the Doppler pattern value table from the base frequency value and an offset.

The offset value is read from the system terminal device, converted to BCD, and then converted to double precision. The Doppler table is then built by successively adding the offset value to the base frequency value and converting the result to packed decimal form.













```

      NMIN(3)=SFREQ
      IF(SFREQ.LT.FREQ)GO TO 30
      NMAX(3)=SFREQ
      NMIN(3)=FREQ
      30 CONTINUE
      C*** INFORM USER THAT OOP TABLE IS BUILT
      WRITE(6,904)
      904 FORMAT(1H,'***OOP TABLE BUILT-SIZE=1024')
      RETURN
      C*** OFFSET SPECIFIED CONTAINED INVALID CHARACTER
      200 WRITE(6,906)
      906 FORMAT(1H,'***INVALID FREQ')
      RETURN
      C*** VALUE NOT IN 0-2 MEGA RANGE GENERATED
      300 WRITE(6,908)
      908 FORMAT(1H,'***FREQ OUT OF RANGE')
      RETURN
      END
  
```

ROUTINES CALLED:  
 SEARCH, NUMBER, ASCRLN, RLNSCU  
 OPTIONS =/ON,/S,/OP:1

BLOCK	LENGTH
DGPD 329	(001222)*
INCP 10	(000024)
MAXIM 24	(000060)
SYSTEM 29	(000072)
TABLES 340	(015700)

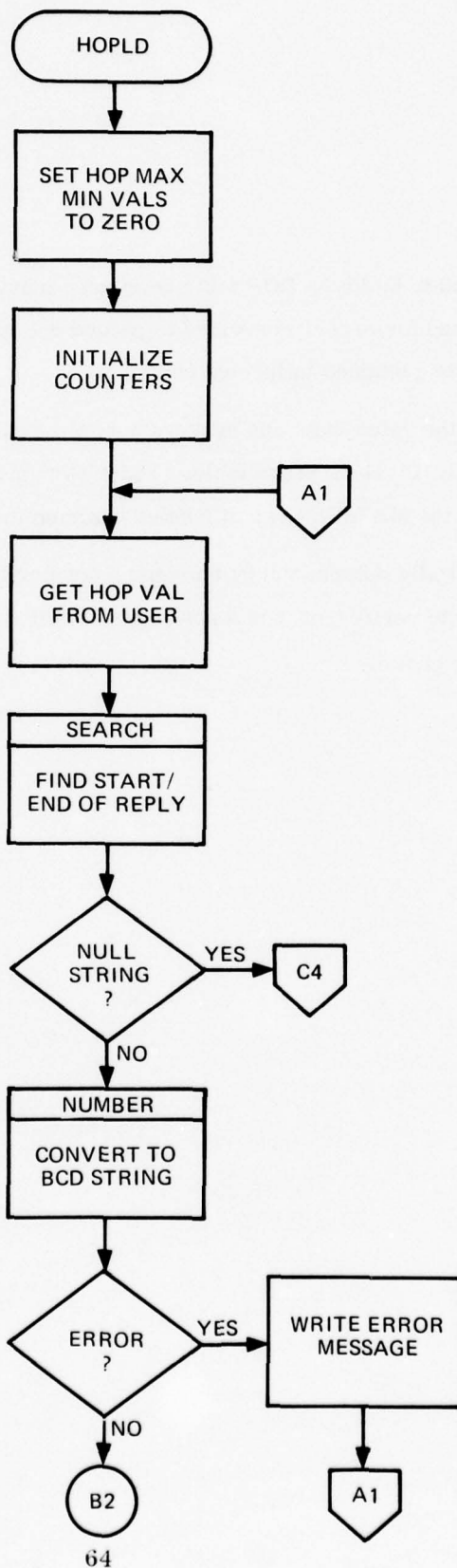
\*\*COMPILER ----- CORE\*\*  
 PHASE USED FREE  
 DECLARATIVES 21522 2304  
 EXECUTABLES 01267 01099  
 ASSEMBLY 01373 06233

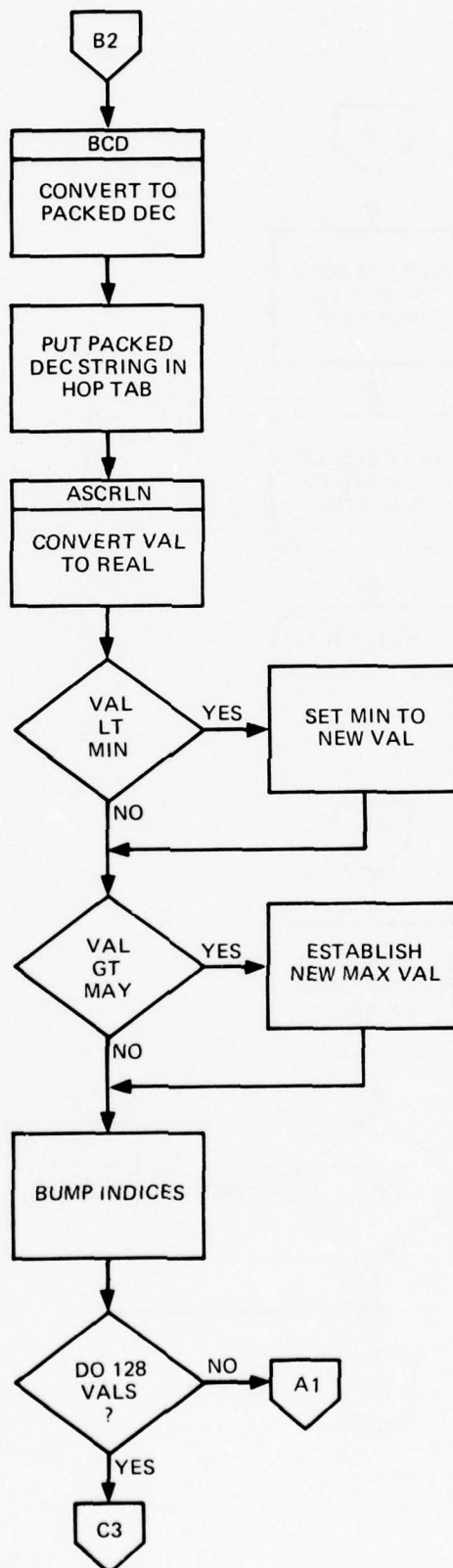
#### SUBROUTINE HOPLD

This routine is used to build the HOP table from user input. Each value input is converted to BCD, checked for error, converted to packed decimal form, and then entered into the HOP table contained in labeled common.

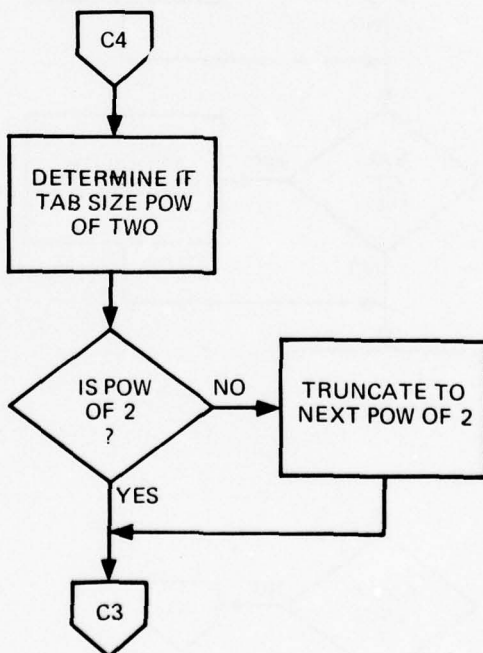
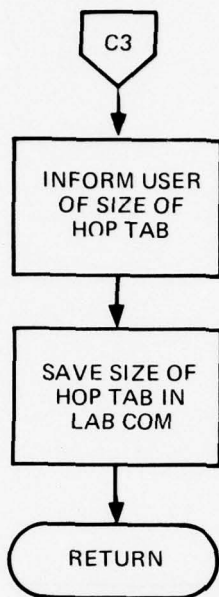
Besides managing the value input and conversions, the routine also determines the maximum and minimum HOP values in the table. These two values, maximum and minimum, are stored in the MAXMIN area of labeled common in double precision form.

The table size, initially determined by bumping a counter after each value is input, is checked before return to verify that it is a power of two. If it is not, the size is truncated to the next closest power of two.









## SUBROUTINE MOPD

```

C*****
C THE PURPOSE OF THIS ROUTINE IS TO BUILD THE MOP TABLE
C USED BY THE INTELL. PATTERNS ARE ALL INPUT FROM THE USER.
C***** TABLE SIZE MUST BE POWER OF TWO OR SIZE IS TRUNCATED.
C*****

```

```

C*****
C BYTE *ORK(5)
C COMMON/I-STOP/INLINE
C COMMON/SYSTEM/START,PSTOP,PCYCLE,PBASE,PSMEND,MASK
C COMMON/TABLES/MOP,DOP,MFSK
C COMMON/MAXMIN/RMAX,RMIN
C DOUBLE PRECISION FREQ,RMAX(3),RMIN(3)
C REAL PSTAT(3),PSTOP(3),PCYCLE(3),PSMEND
C INTEGER MASK(3)
C BYTE INLINE(20),IVAL(12),PBASE(12)
C BYTE MOP(540),DOP(5120),MFSK(320)
C RMAX(1)=2.0
C RMIN(1)=0.0
C ISAVE=128
C J=1

```

```

I=1
C**** QUERY FOR PATTERN I
10 WRITE(6,9.0)I
900 FORMAT(1H,"MOP FREQ('",I3,'") =',/)
C**** HEAD USER REPLY
902 FORMAT(22A1)
HEAD(6,902)INLINE
C**** FIND START AND END OF REPLY
CALL SEARCH(ISTART,IEND)
IF(ISTART.EQ.0)GO TO 220
CONVERT TO BCD STRING
CALL NUMBER(ISTART,IEND,IVAL,IERR)
IF(IERR.NE.0)GO TO 20
FREQ INPUT CONTAINS BAD CHARACTER
WRITE(6,9.0)I
904 FORMAT(1H,"***INVALID FREQ")
GO TO 10
C**** CONVERT TO 5 BYTE INTELL FORM
20 CALL BCD(IVAL,WORK)
C**** PUT IN MOP TABLE
DO 23 K=1,5
MOP(J)=WORK(K)
J=J+1
23 CONTINUE
I=I+1
C**** CHECK FOR MAX/MIN INPUT FREQ THIS PATTERN
CALL ASCRN(IVAL,FREQ)
IF(FREQ.LT.RMIN(1))RMIN(1)=FREQ
IF(FREQ.GT.RMAX(1))RMAX(1)=FREQ
C**** MOP TABLE LESS THAN EQUAL TO 120
IF(I.LE.120)GO TO 10
C**** INFORM USER OF SIZE OF MOP TABLE
25 WRITE(6,9.0)ISAVE

```

```

906 FORMAT(1H, '***TOP TABLE BUILT-SIZE=', I5)
C*** SAVE TABLE SIZE IN COMMON FOR PAT MASK GENERATION
MASK(1)=1,SAVE
RETURN

```

```

C*** DETERMINE IF SIZE IS POWER OF TWO
200 I=1
DO 230 K=1,8
M=2**K
IF(M-1)210,210,230
210 ISAVE=M
230 CONTINUE
IF(I.EQ.0)ISAVE=1
GO TO 25
END

```

ROUTINES CALLED:  
SEARCH, NUMBER, BCD , ASCRLN

OPTIONS =/ON,/SU,/OP:1

BLOCK	LEN:TH
HOPLO 334	(001230)*
INSUF 10	(000020)
SYSTEM 20	(000072)
TABLES 3040	(013700)
MAXMIN 20	(000060)

```

**COMPILE --- CORE**
PHASE USED FREE
DECLARATIVES 00-22 02304
EXECUTABLES 01-67 01899
ASSEMBLY 0129 06177

```

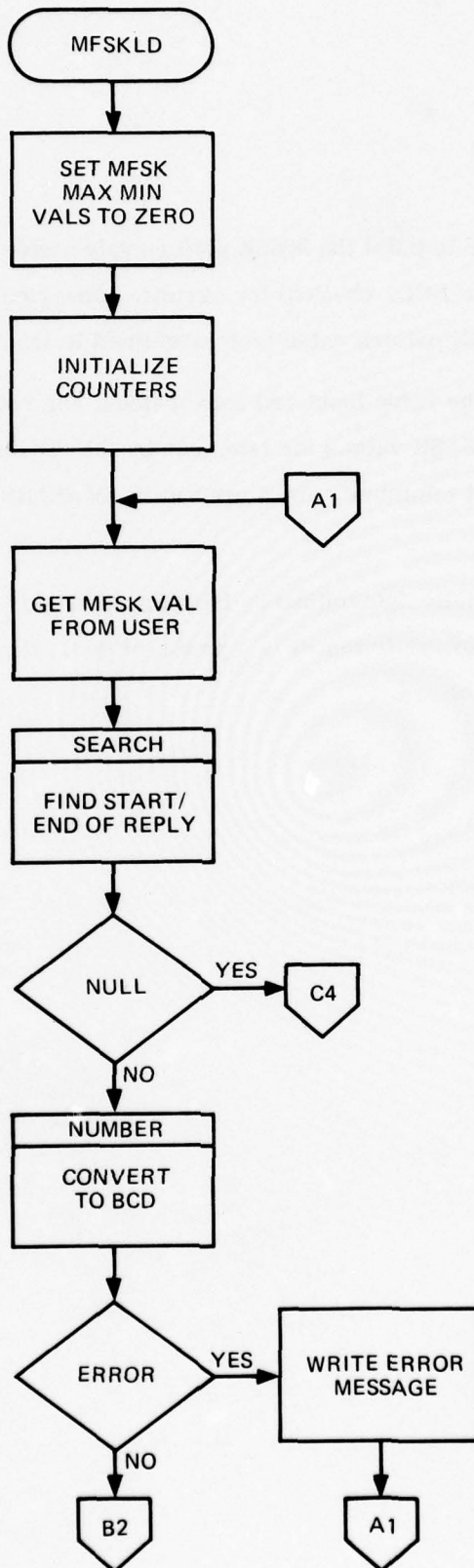
#### SUBROUTINE MFSKLD

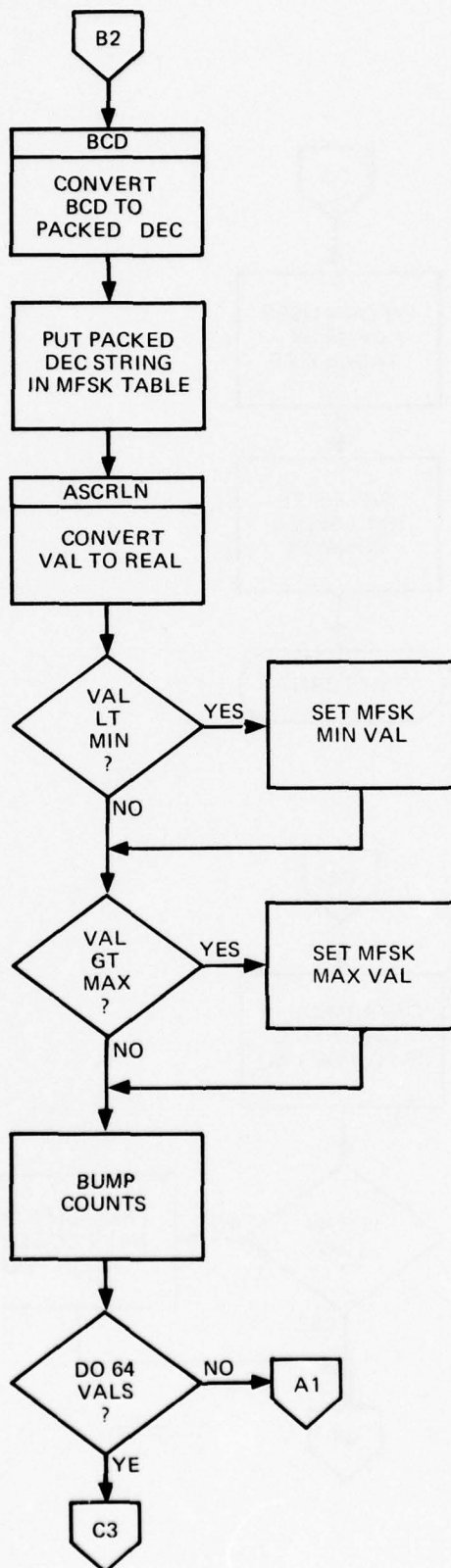
This routine is used to build the MFSK pattern value table from user input. Each value input is converted to BCD, checked for errors, converted to packed decimal, and then entered into the MFSK pattern value table contained in labeled common.

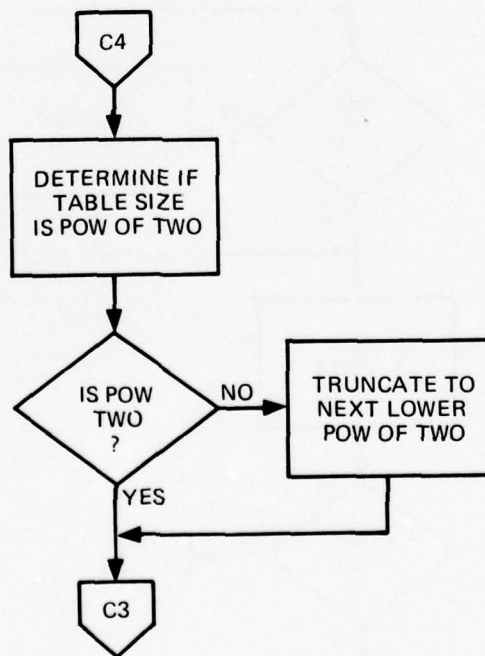
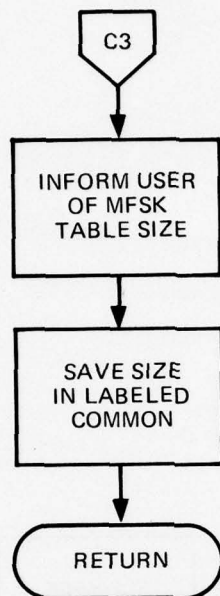
Besides managing the value input and conversions, the routine also determines the maximum and minimum MFSK values for later use by the "INTELL" routine. These two values, maximum and minimum, are stored in the MAXMIN area of labeled common in double precision form.

The table size, initially determined by bumping a counter after each value is input, is checked before return to verify that it is a power of two. If not, the size is truncated to the next closest power of two.













```

25  WRITE(6,906)ISAVE
906  FORMAT(1H, '*****MFSK TABLE BUILT-SIZE=',I5)
C***  SAVE TABLE SIZE IN COMMON FOR PAT MASK GENERATION
      MASK(2)=ISAVE
      RETURN
200  I=I-1
C***  DETERMINE IF SIZE IS POWER OF TWO ADJUST IF NOT
      DO 230 K=1,7
          M=2**K
          IF(M-I)210,210,230
210  ISAVE=M
230  CONTINUE
      IF(I.EQ.0)ISAVE=1
      GO TO 25
      END

```

ROUTINES CALLED:  
SEARCH, NUMBER, RCD , ASCRLN

OPTIONS =/ON,/SU,/OP:1

BLOCK	LENGTH
MFSKLD 336	(001240)*
INBUF 10	(000024)
SYSTEM 29	(000072)
TABLES 3040	(013700)
MAXMIN 24	(000060)

```

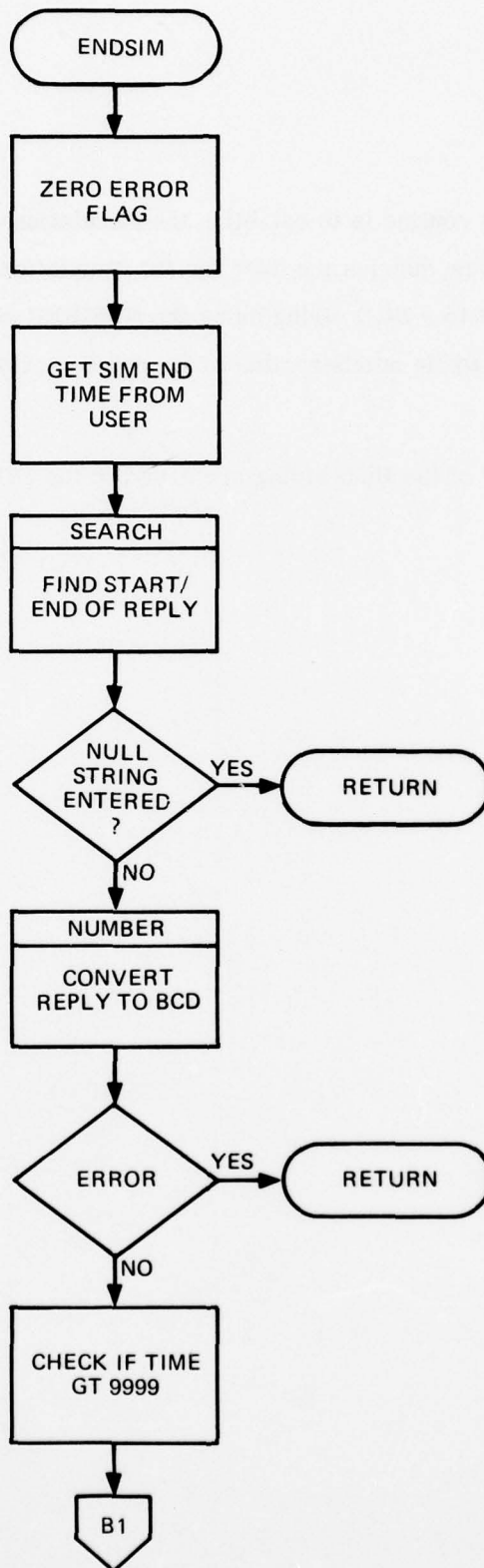
**COMPILER ----- CODE**
PHASE USED FREE
DECLARATIVES 00522 02344
EXECUTABLES 01067 01899
ASSEMBLY 01437 06169

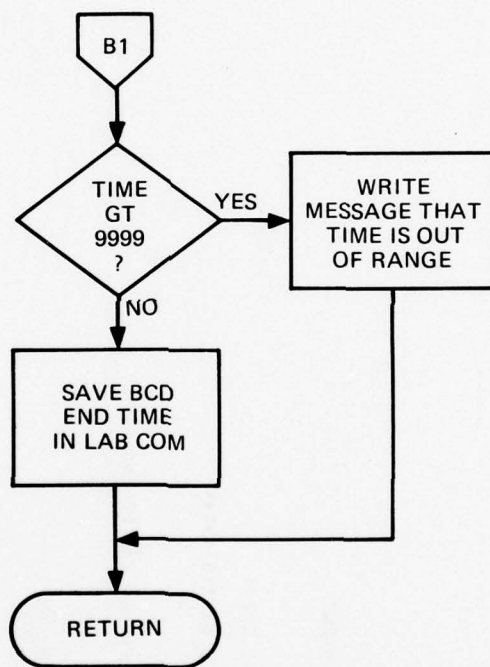
```

#### SUBROUTINE ENDSIM

The purpose of this routine is to establish the simulation duration or end time via operator input. The routine queries the user for the simulation end time value, reads the reply, and converts it to a BCD string using the NUMBER subroutine. The converted value is interpreted as a whole number value of the number of minutes to run the simulation.

Bytes 5, 6, 7 and 8 of the BCD string are saved in the SYSTEM labeled common area.







```

SUBROUTINE END5IM(IERR)
C*****
C THE PURPOSE OF THIS ROUTINE IS TO ESTABLISH THE SIMULATION
C END TIME FROM OPERATOR INPUT. END TIME IS SPECIFIED IN MINUTES.
C THE VALUE INPUT AFTER CONVERSION TO BCD IS SAVED IN COMMON.
C*****
COMMON/IN-UP/INLINE
      BYTE INLINE(20)
      COMMON/SYSTEM/START, PSTOP, PCYCLE, PHASE, PSMEND
      REAL PSTART(3), PSTOP(3), PCYCLE(3), PSMEND
      BYTE PHASE(12), IVAL(12)
      EQUIVALENCE (ASCII, IVAL(5))
C*** WRITE QUERY MESSAGE
      WRITE(6,*)
      800 FORMAT(1H, 'END TIME =',/)
C*** GET REPLY
      READ(5,*)
      302 FORMAT(20A1)
      IERR=0
C*** DETERMINE START AND END OF REPLY
      CALL SEARCH(ISTART, IEND)
      IF(ISTART.EQ.0) RETURN
      CONVERT TO BCD STRING
      CALL NUMBER(ISTART, IEND, IVAL, IERR)
      IF(IERR.NE.0) RETURN
C*** VALUE SHOULD NOT BE GT 4 BCD DIGITS(9999)
      DO 20 I=2,4
        IF(IVAL(I).NE.0) GO TO 50
      20 CONTINUE
C*** ASCII EQUIV TO IVAL(5) RETURN BCD VAL OF END
      PSMEND=ASCII
      RETURN
      50 WRITE(6,*)
      900 FORMAT(1H, '***TIME OUT OF RANGE')
      RETURN
      END

ROUTINES CALLED:
SEARCH, NUMBER

OPTIONS =/ON,/SU,/OP:1

BLOCK      LENGTH
END5IM      161      (000502)*
IABUF      10      (000220)
SYSTEM      26      (000664)

**COMPILER ***** CODE**
PHASE      USED FREE
DECLARATIVES 02315 02151
EXECUTABLES 00463 02103
ASSEMBLY    01127 06419

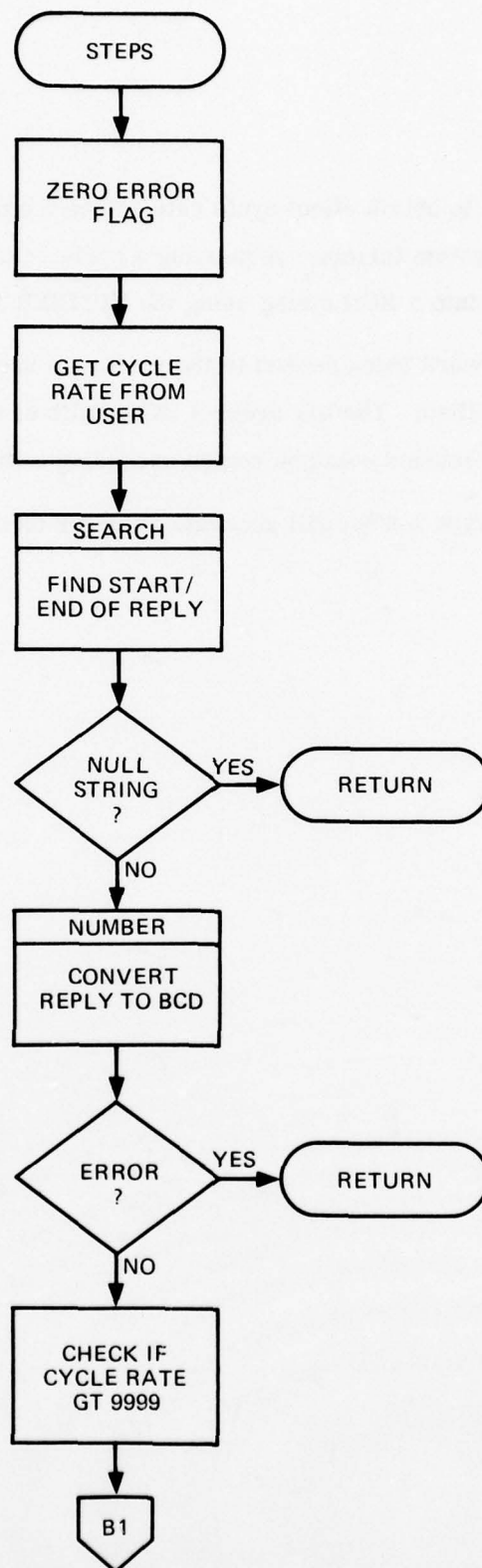
```

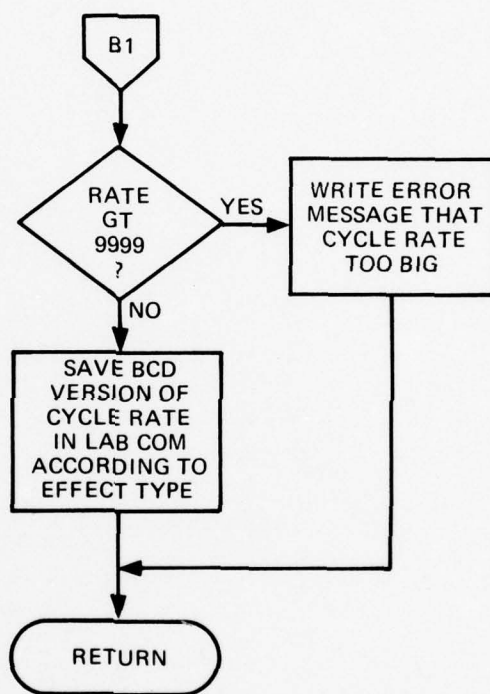
#### SUBROUTINE STEPS

This routine is used to obtain effect cycle rate values from the user. The routine writes a message to the system terminal requesting a cycle value be provided, reads the reply, and converts it into a BCD string using the NUMBER routine.

The value of the keyword index passed to the routine is used to determine the particular effect type specified. The low order 4 BCD digits of the converted string are stored in the SYSTEM labeled common region according to the effect type determined.

A value not in the range 0-9999 will generate an error message.







SUBROUTINE STEPS(IND,IERR)  
C \*\*\*\*\*

C \*\*\*\*\* THE PURPOSE OF THIS ROUTINE IS TO ESTABLISH THE CYCLE  
C \*\*\*\*\* RATE THROUGH OPERATOR INPUT. THE VALUE IND DETERMINES WHICH  
C \*\*\*\*\* CYCLE RATE IS INPUT(13=HOP,14=HFSK,15=HOPP).THE VALUE AFTER HCO  
C \*\*\*\*\* CONVERSION. IS SAVED IN THE PCYCLE AREA OF COMMON.  
C \*\*\*\*\*

C \*\*\*\*\*  
C \*\*\*\*\* COMMON/INOUT/INLINE  
C \*\*\*\*\*

BYTE IN(1)=E(24)  
COMMON/SYSTEM/START,STOP,PCYCLE,PHASE,PSHEND,MASK  
REAL PSTART(3),PSTOP(3),PCYCLE(3),PSHEND,ASCII  
BYTE PHASE(12),IVAL(12)  
INTEGER MASK(3)  
EQUIVALENCE (ASCII,IVAL(5))  
IERR=0

C \*\*\*\*\* ASK FOR CYCLE RATE  
C \*\*\*\*\* WRITE(6,F4.0)  
C \*\*\*\*\* FORMAT(1F,\*,CYCLE RATE \*,/)

800  
C \*\*\*\*\* READ REPLY,  
C \*\*\*\*\* READ(6,F4.0)INLINE  
802 FORMAT(2F4.0)

C \*\*\*\*\* GET REPLY START AND END  
C \*\*\*\*\* CALL SEARCH(ISTART,IEND)  
C \*\*\*\*\* IF(ISTART.EQ.0)RETURN

C \*\*\*\*\* CONVERT REPLY TO HCO STRING  
C \*\*\*\*\* CALL NUMBER(ISTART,IEND,IVAL,IERR)  
C \*\*\*\*\* IF(IERR.NE.0)RETURN

C \*\*\*\*\* RATE MUST NOT EXCEED 9999  
C \*\*\*\*\* DO 20 I=2,4  
C \*\*\*\*\* IF(IVAL(I).NE.0)GO TO 50  
C \*\*\*\*\* CONTINUE

20  
C \*\*\*\*\* INSERT CYCLE RATE ACCORDING TO IND VAL  
C \*\*\*\*\* PCYCLE(IND)=IVAL  
C \*\*\*\*\* RETURN

50  
900  
C \*\*\*\*\* WRITE(6,F4.0)  
C \*\*\*\*\* FORMAT(1F,\*,\*\*CYCLE RATE TOO LARGE\*)  
C \*\*\*\*\* RETURN  
C \*\*\*\*\* END

ROUTINES CALLED:  
SEARCH, NUMBER

OPTIONS =/ON,/SU,/UP/1

BLOCK	LENGTH
STEPS 170	(200524)*
INDUP 10	(200224)
SYSTEM 29	(200272)

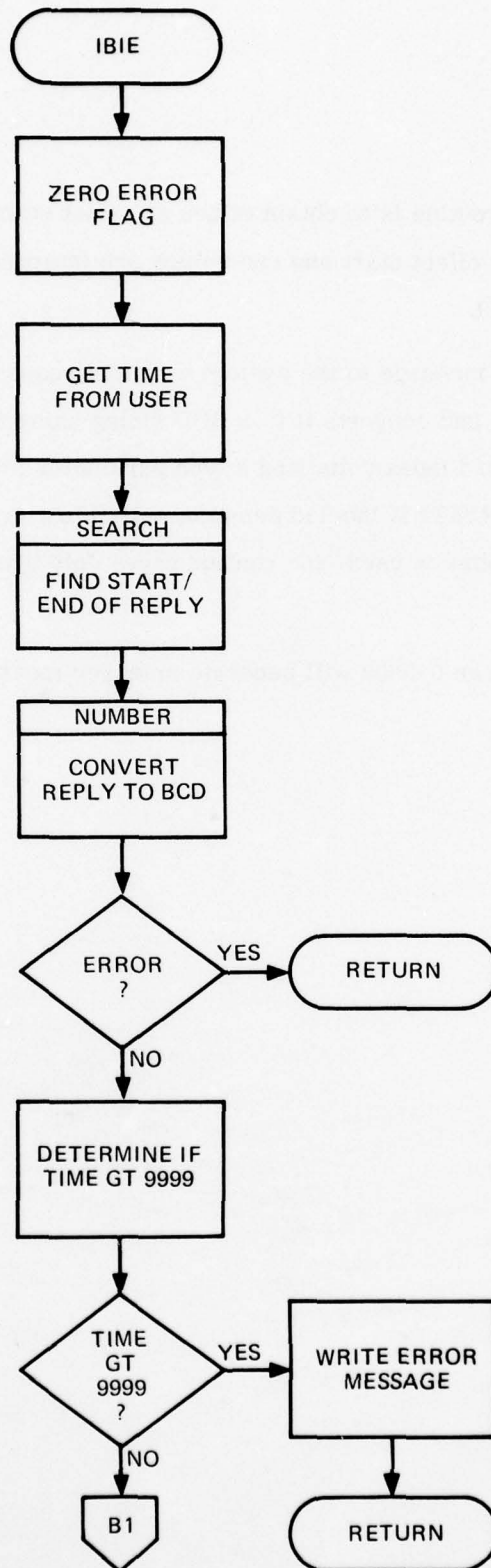
\*\*COMPILER \*\*\*\*\* COME\*\*  
PHASE USED FREE  
DECLARATIVES 00-22 02304  
EXECUTABLES 00-96 02070  
ASSEMBLY 21215 06391

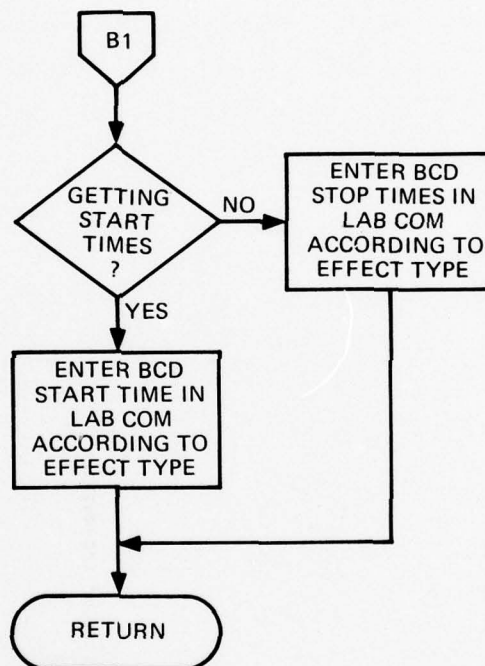
#### SUBROUTINE IBIE

The purpose of this routine is to obtain either an effect start or effect end time value from the user. Both effect start and end values are interpreted as whole number minutes in the range 0-9999.

The routine writes a message to the system terminal requesting a time value be provided, reads the reply, and converts it to a BCD string using the NUMBER subroutine. The routine uses the keyword index value and a type parameter (either STOP or START) to determine where in the SYSTEM labeled common region to store the value. Since only a four digit whole number is used, the routine saves only bytes 5, 6, 7, and 8 of the converted BCD string.

A value not in the range 0-9999 will generate an error message.







```

SUBROUTINE I0IE(IND,TYPE,IERR)
C*****
C THE PURPOSE OF THIS ROUTINE IS TO ESTABLISH EITHER THE
C EFFECT START OR END TIMES THROUGH OPERATOR INPUT. THE
C TYPE PARAMETER DETERMINES STOP OR START. IND DETERMINES
C WHICH EFFECT. IND=7,11 IS HUP, 8,11 IS MFSK, 9,12 IS UOP. THE
C VALUE AFTER BCD CONVERSION IS SAVED IN EITHER THE PSTART OR
C PSTOP AREAS OF LABELED COMMON.
C*****
COMMON/INUP/INLINE
BYTE INLINE(20)
COMMON/SYSTEM/PPSTART,PPSTOP,PCYCLE,PBSE,PBSEND,MASK
REAL PSTART(3),PPSTOP(3),PCYCLE(3),PBSEND,ASCII
BYTE PBSE(12),IVAL(12)
INTEGER MASK(3)
EQUIVALENCE (IVAL(5),ASCII)
IERR=0
C***** QUERY FOR TIME
C***** WRITE(6,ROW)
800 FORMAT(1X, 'TIME(MINS) =',/)
C***** READ USER REPLY
READ(6,ROW)INLINE
802 FORMAT(2X,1)
C***** GET START AND END OF REPLY
CALL SEARCH(ISTART,IEND)
IF(ISTART.EQ.0)RETURN
CONVERT REPLY TO BCD STRING
CALL NUMBER(ISTART,IEND,IVAL,IERR)
IF(IERR.GT.0)GO TO 200
C***** VALUE MUST BE LE 9999
DO 20 I=2,4
IF(IVAL(I).NE.0)GO TO 100
CONTINUE
20 DETERMINE IF START OR STOP AND SAVE VALUE ACCORDINGLY
IF(TYPE.EQ.'STOP')GO TO 50
INDEX=IND-6
C***** ASCII IS BYTES 5-8 OF IVAL
PSTART(INDEX)=ASCII
RETURN
50 INDEX=IND-9
C***** ASCII IS BYTES 5-8 OF IVAL
PSTOP(INDEX)=ASCII
RETURN
100 WRITE(6,940)
900 FORMAT(1X, '***TIME OUT OF LIMITS**')
RETURN
200 IERR=1
RETURN
END
ROUTINES CALLED:
SEARCH, NUMBER
OPTIONS =/ON,/SU,/OP:1
ALCK LENGTH

```

FORTRAN V06.13

00:11:00

21-JAN-70

PAGE

2

IRIE 005 (000532)\*  
INBUF 10 (000024)  
SYSTEM 29 (000072)

\*\*COMPILER ----- CODE\*\*  
PHASE USED FREE  
DECLARATIVES 00022 02344  
EXECUTABLES 00496 02070  
ASSEMBLY 01247 06359

#### SUBROUTINE FREQ

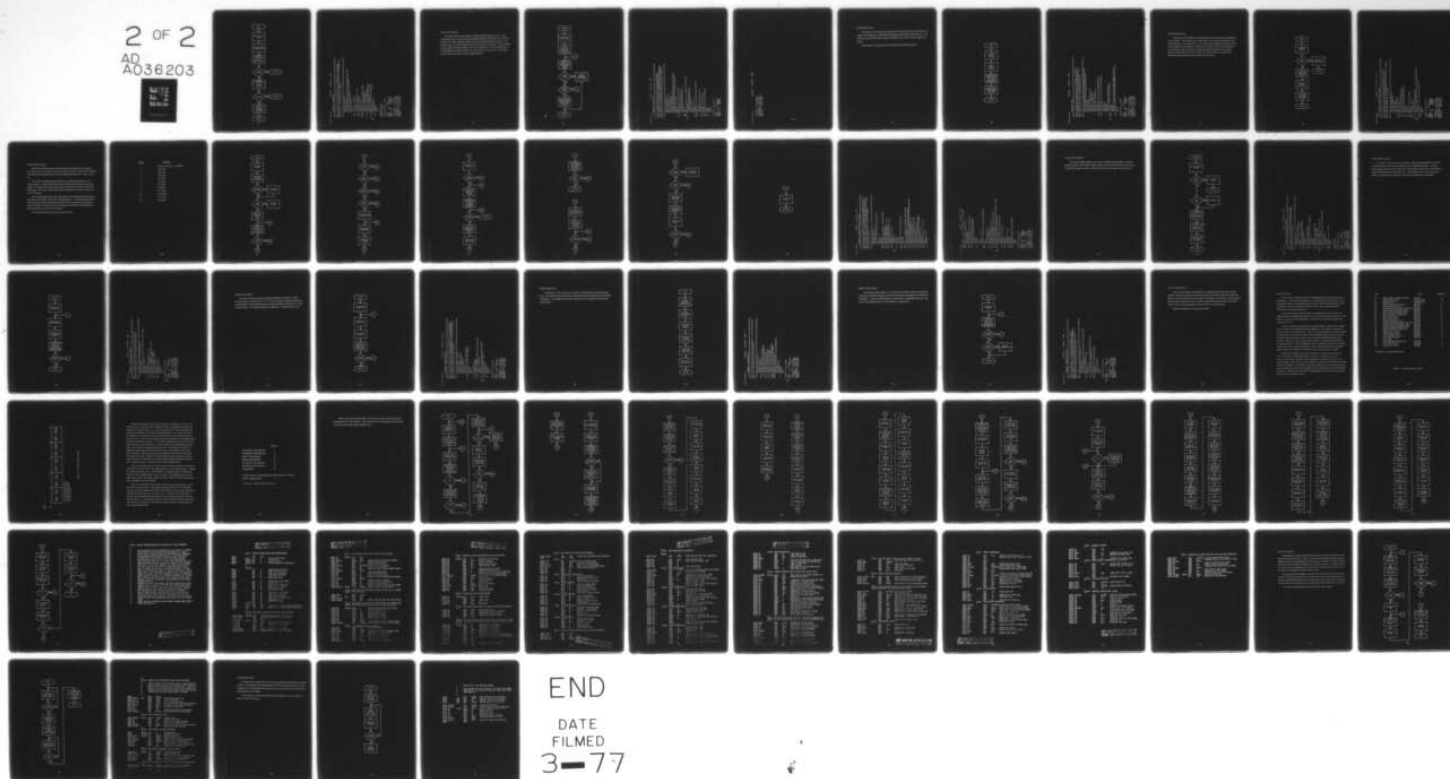
This routine is used to obtain the base frequency value from the user. The routine writes a message to the system terminal requesting a base frequency value be provided, reads the reply, and converts it to a BCD string using the NUMBER subroutine. The BCD value of the base frequency is then stored in labeled common.

AD-A036 203

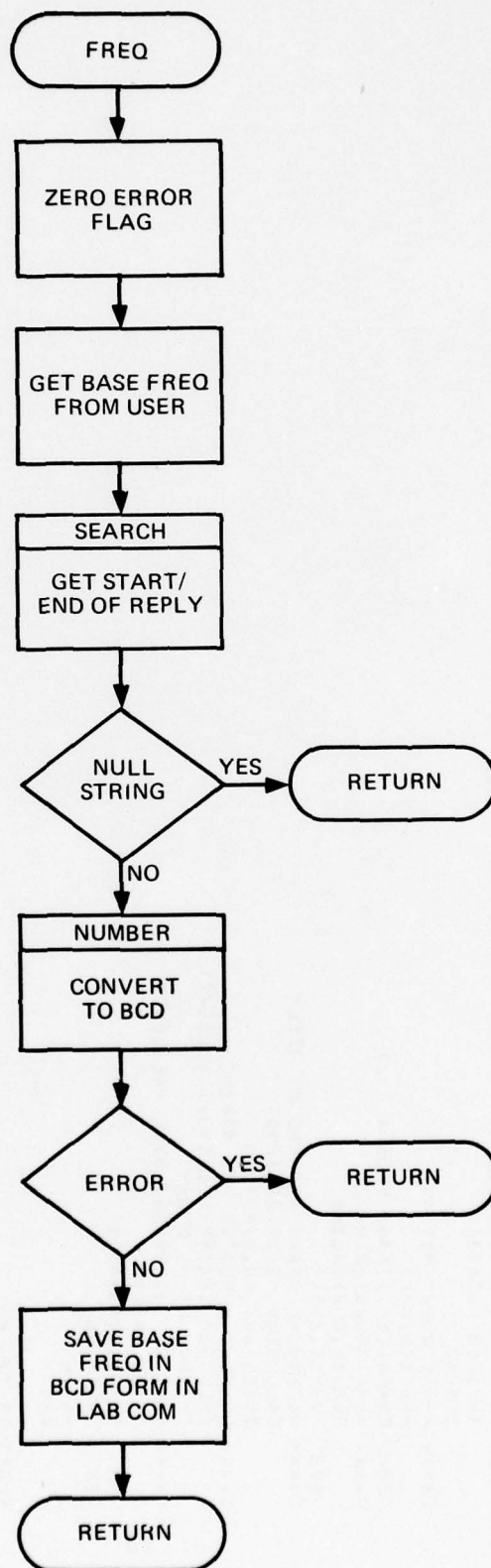
COMPUTER SCIENCES CORP FALLS CHURCH VA F/G 9/2  
CSEL INTERFACE UPDATE: K-BAND MICROPROCESSOR DEMONSTRATION.(U)  
DEC 76 D O ALWINE, R A GLICKSMAN, R G MURRAY F33615-75-C-1229  
CSC-R-3328-1 AFAL-TR-76-169 NL

UNCLASSIFIED

2 OF 2  
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A036203







```

SUBROUTINE FREQ(IERR)
C*****
C
C**** THE PURPOSE OF THIS ROUTINE IS TO ESTABLISH THE BASE FREQ
C**** THROUGH OPERATOR INPUT. THE FREQ VALUE AFTER BCD CONVERSION IS
C**** SAVED IN THE PBASE AREA OF COMMON.
C
C*****
COMMON/INBUF/INLINE
BYTE INLINE(20)
COMMON/SYSTEM/PSSTART,PSTOP,PCYCLE,PBASE,PSMEND,MASK
REAL PSSTART(3),PSTOP(3),PCYCLE(3),PSMEND
BYTE PBASE(12),IVAL(12)
INTEGER MASK(3)
IERR=0
C**** WRITE QUERY MESSAGE
WRITE(6,*)
SWM FORMAT(3H,'BASE FREQ = ',/)
C**** READ OPERATOR REPLY
READ(6,802)INLINE
802 FORMAT(20A1)
C**** DETERMINE START AND END OF REPLY
CALL SEARCH(ISTART,IEND)
IF(ISTART.EQ.0)RETURN
CALL NUMBER(ISTART,IEND,IVAL,IERR)
IF(IERR.GT.0)RETURN
C**** SAVE BCD STRING AS BASE FREQUENCY
DO 20 I=1,12
  PBASE(I)=IVAL(I)
20 CONTINUE
RETURN
END

```

90

ROUTINES CALLED:  
SEARCH, NUMBER

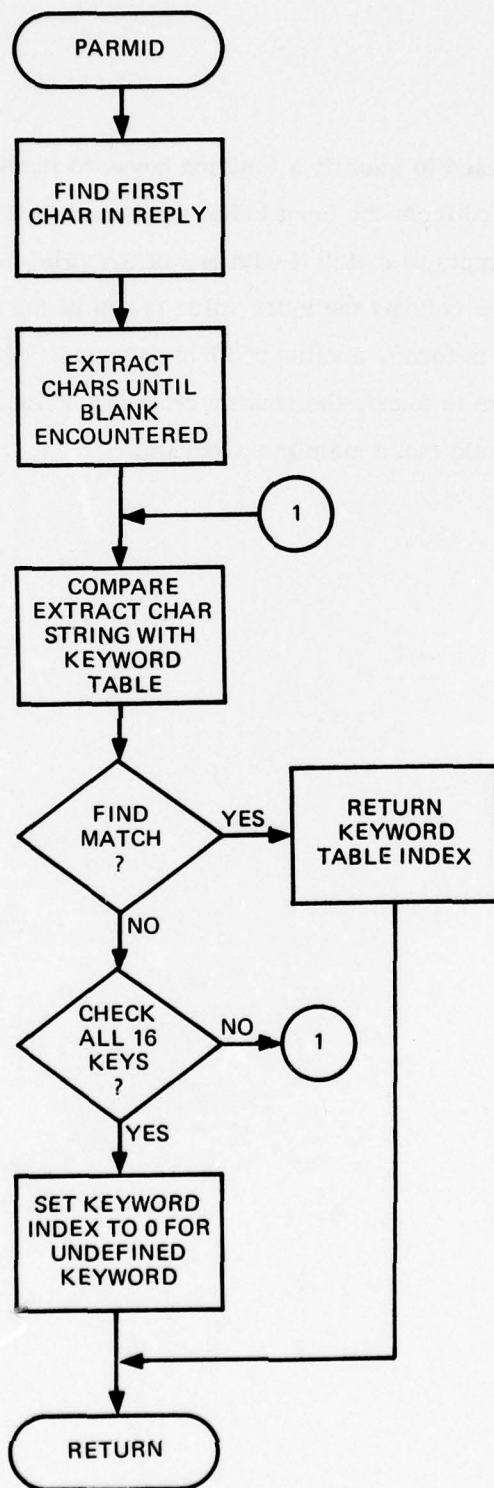
OPTIONS =/ON,/SU,/OP:1

BLOCK	LENGTH
FREQ	127 (000376)*
INBUF	10 (000020)
SYSTEM	29 (000072)

\*\*COMPILER ---- CORE\*\*  
 PHASE USED FREE  
 DECLARATIVES 00022 02344  
 EXECUTABLES 00086 02080  
 ASSEMBLY 01127 06479

#### SUBROUTINE PARMID

This subroutine is used to identify a function keyword input by the user. After extracting the user keyword from the input buffer contained in the INBUF area of labeled common, the routine attempts to match it with one of the valid function keywords. If a match is found, the routine returns the index value (1-16) of the keyword. If a null string, carriage return response is found, a value of 17 is returned. If a non-carriage return and unidentifiable response is found, the routine returns a value of zero. The routine is called only from the static mode mainline program.





```

SUBROUTINE PARMID(IND)
C*****
C**** THE PURPOSE OF THIS ROUTINE IS TO IDENTIFY THE USER
C**** SPECIFIED KEYWORD AND RETURN A NUMERIC IDENTIFIER TO
C**** THE CALLER. THE IDENTIFIER IND CORRESPONDS TO THE INDEX OF THE
C**** KEYWORD IN THE PARM ARRAY. IND IS 0 IF THE KEYWORD CAN NOT BE
C**** FOUND AND IS NOT A CAR RETN. IND=17 WHEN EQUAL TO CAR RETN.
C
C*****
COMMON/INBUF/INLINE
COMMON/SPCODEC/CHANS,ICAR
BYTE CHANS(20)
BYTE INL1E(20),ABYT(4)
REAL PARM3(16),ASCII
EQUIVALENCE (ASCII,ABYT(1))
DATA PARM3/'SHOW','LOAD','FREQ','HOPL','MFSL','DOPL',
1 'HSTR','NSTR','DSTR','HEND','MEND','OEND','HCYC',
2 'HCYC','DCYC','SEND',
ASCII/
C**** SCAN FOR FIRST CHARACTER IN REPLY
DO 10 I=1,20
IF (INLINE(I).EQ.ICAR)GO TO 70
IF (INLINE(I).NE.CHARS(7))GO TO 15
10 CONTINUE
15 K=1
C**** FILL THE ABYT ARRAY WITH CHARS UNTIL END STRING
DO 20 J=1,20
IF (INLINE(J).EQ.ICAR)GO TO 30
IF (INLINE(J).EQ.CHARS(7))GO TO 30
ABYT(K)=INLINE(J)
K=K+1
IF (K.GT.4)GO TO 30
20 CONTINUE
C**** ABYT EQUIV TO ASCII=MATCH ASCII WITH KEYS
30 INDS=
DO 40 I=1,16
IF (PARMS(I).EQ.ASCII)GO TO 60
40 CONTINUE
C**** NO MATCH THAN IND IS ZERO
RETURN
C**** FOUND MATCH SET IND ACCORDINGLY
60 IND=I
RETURN
70 IND=17
RETURN
END

```

OPTIONS =/ON,/SU,/OP:1

BLOCK	LENGTH
PARMID 206	(000034)*
INBUF 10	(000024)
SPCODEC 11	(000026)

FORTHAN V06.15

00:12:59

21-JAN-76

PAGE

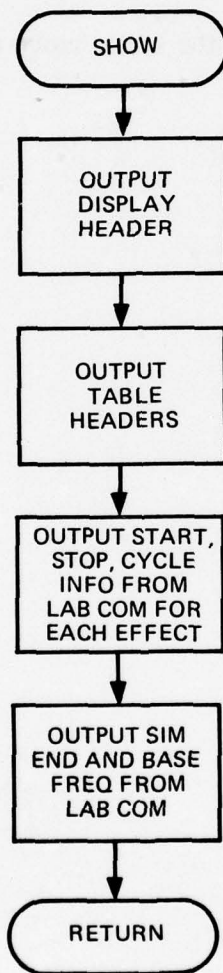
2

\*\*COMPILER ----- CORE\*\*  
PHASE USED FREE  
DECLARATIVES 00522 02344  
EXECUTABLES 00592 02074  
ASSEMBLY 01107 06099

#### SUBROUTINE SHOW

The purpose of this routine is to display the current effect start, end, and cycle values, base frequency, and simulation end value on the system terminal device. The values are stored in the labeled common SYSTEM area in BCD form and output in "T" format.

This routine is called only from the static mode mainline program.





```

C***** THE PRUPOSE OF THIS ROUTINE IS TO DISPLAY THE CURRENT
C***** SYSTEM PARAMETERS TO THE USER. THE PARAMETERS ARE
C***** INITIALIZED IN BLOCK DATA AND SET BY THE USER. THEIR
C***** CURRENT VALUE ARE IN LABELED COMMON(SYSTEM).
C
C*****
COMMON/SYSTEM/PSTART,PSTOP,PCYCLE,PHASE,PSMEND,MASK
REAL PSTART(3),PSTOP(3),PCYCLE(3),PSMEND,ID(3)
BYTE PHASE(12)
INTEGER MASK(3)
BYTE ABYT(4),BMYT(4),CBYT(4)
EQUIVALENCE (ABYT(1),A)
EQUIVALENCE (B,BMYT(1))
EQUIVALENCE (C,CMYT(1))
DATA ID/'NOP ','MASK','DOP '/
WRITE(6,8140)
800  FORMAT(1H ,2X,'*****SYSTEM PARAMETERS*****')
WRITE(6,8142)
902  FORMAT(1H ,8X,'START',5X,'END ',4X,'CYCLE')
DU 20 1=1,3
A=PSTART(1)
B=PSTOP(1)
C=PCYCLE(1)
WRITE(6,9144)ID(1),ABYT,8BMYT,CMYT
904  FORMAT(1H ,A4,4X,4I1,5X,4I1,5X,4I1)
20  CONTINUE
A=PSMEND
WRITE(6,9146)ABYT,(PHASE(J),J=2,8),(PHASE(K),K=9,11)
906  FORMAT(1H ,51M ENDS ',4I1,2X,'BASE FREQ=',7I1,' ',3I1)
RETURN
END

```

OPTIONS =/ON,/SU,/OP:1

BLOCK	LENGTH
SHOW	244 (000750)*
SYSTEM	29 (0000072)

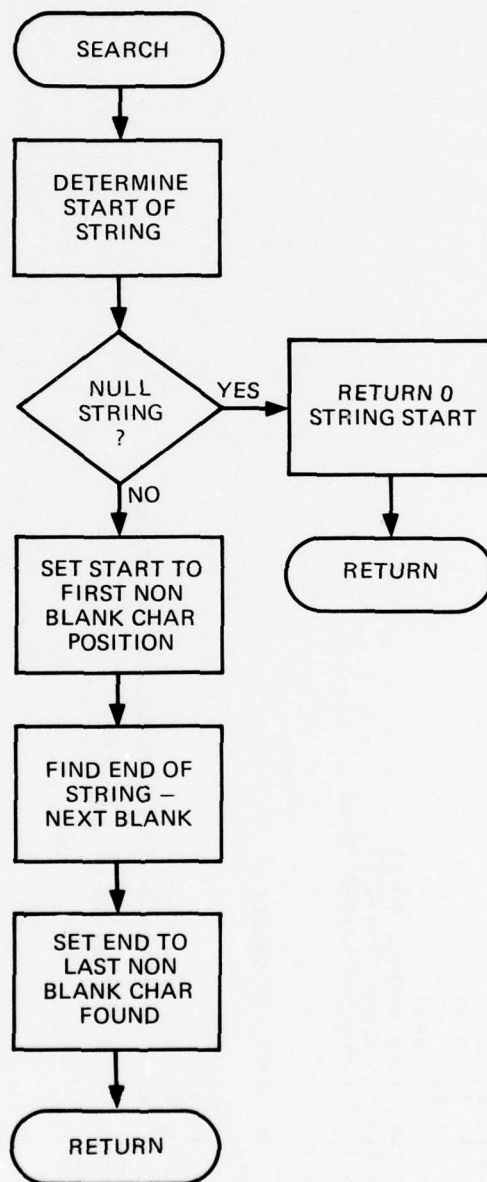
```

**COMPILER ---- CORE**
      PHASE      USED  FREE
DECLARATIVES 00027 02139
EXECUTABLES  00063 02103
ASSEMBLY      01222 06384

```

#### SUBROUTINE SEARCH

The purpose of this routine is to determine the start and end character positions of a user response. The routine first scans the INBUF area of labeled common for a non-blank character or a carriage return. If a carriage return is found, the routine sets the start parameter to zero and exits. Otherwise, the routine sets the start parameter to the character position of the first non-blank character and continues its scan until a blank or carriage return character is found. The end parameter is then set to the character position of the blank or carriage return character.



```

      SUBROUTINE SEARCH(ISTART,IEND)
      C*****
      C
      C**** THE PURPOSE OF THIS ROUTINE IS TO DETERMINE THE START
      C**** AND END POSITION IN THE INLINE ARRAY OF THE USERS
      C**** RESPONSE. ISTART IS THE BEGINNING, IEND IS THE FINISH. ISTART=0
      C**** WILL INDICATE A CAR RETN REPLY.
      C
      C*****
      C*****
      COMMON/SPCDEC/CHARS,ICAR
      COMMON/INBUF/INLINE
      BYTE CHARS(20)
      C**** DETERMINE THE START
      DO 20 I=1,20
      C**** CHECK FOR CAR RETN
      IF(INLINE(I).EQ.ICAR)GO TO 25
      C**** CHECK FOR NIN BLANK CHARACTER
      IF(INLINE(I).NE.CHARS(7))GO TO 30
      20 CONTINUE
      25 ISTART=0
      RETURN
      C**** ESTABLISH START FOR CALLER
      30 ISTART=1
      C**** FIND END POSITION
      DO 50 J=1,20
      C**** CHECK FOR BLANK OR CAR RETN
      IF(INLINE(J).EQ.CHARS(7).OR.INLINE(J).EQ.ICAR)GO TO 60
      50 CONTINUE
      C**** END IS ONE LESS THAN BLANK OR CAR RETN
      60 IEND=J-1
      RETURN
      END

```

100

OPTIONS =/ON,/SU,/OP:1

BLOCK	LENGTH
SEARCH 99	(000326)*
SPCDEC 11	(000026)
INBUF 10	(000024)

```

**COMPILER ----- CORE**
PHASE USED FREE
DECLARATIVES 00002 02164
EXECUTABLES 00783 02183
ASSEMBLY 00995 06611

```



#### SUBROUTINE NUMBER

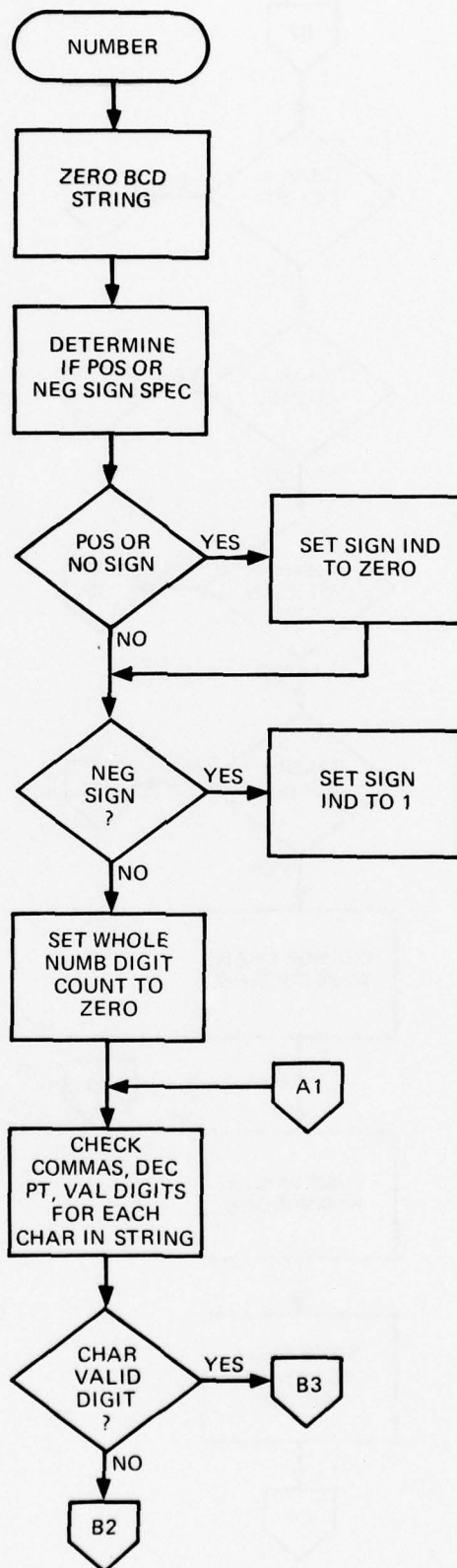
Subroutine NUMBER is called by all subroutines performing operator dialogue. Its purpose is to scan a response string to verify that it contains a valid numeric response and to build a BCD equivalent array for use in determining frequencies, values, times, etc.

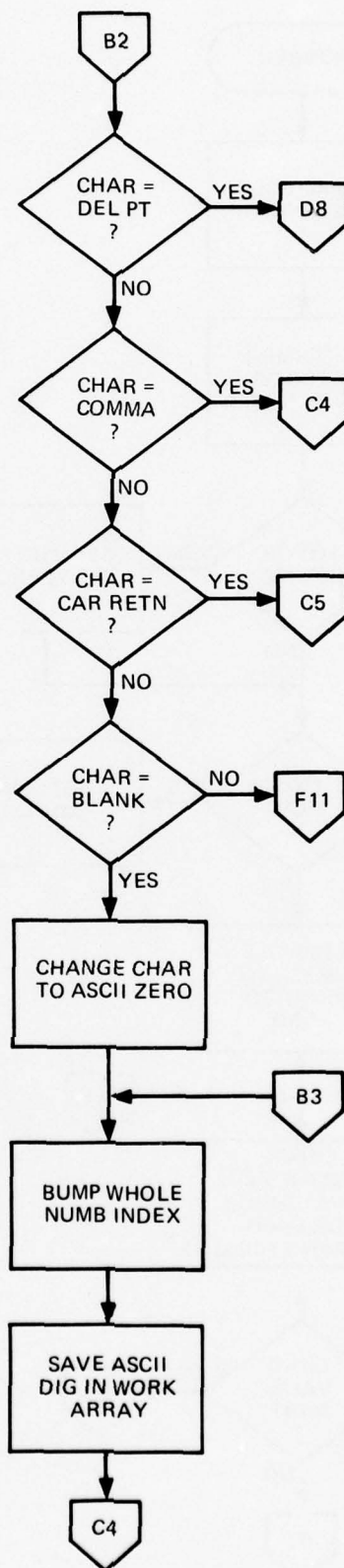
The response string scanned by the routine is contained in the INBUF area of labeled common. The start and end character positions in the string are passed to the routine. The routine will accept a sign, comma, decimal point, or blank as part of the input string. Any other non ASCII digit character contained in the string is considered an error condition.

After determining the sign value of the response, the routine begins extracting the ASCII digits of the whole number value of the input string. If a decimal point is encountered, the routine begins extracting the fractional part of the string and converting it to its BCD equivalent. Conversion of the whole number ASCII digits to their BCD equivalents is performed prior to return to the caller.

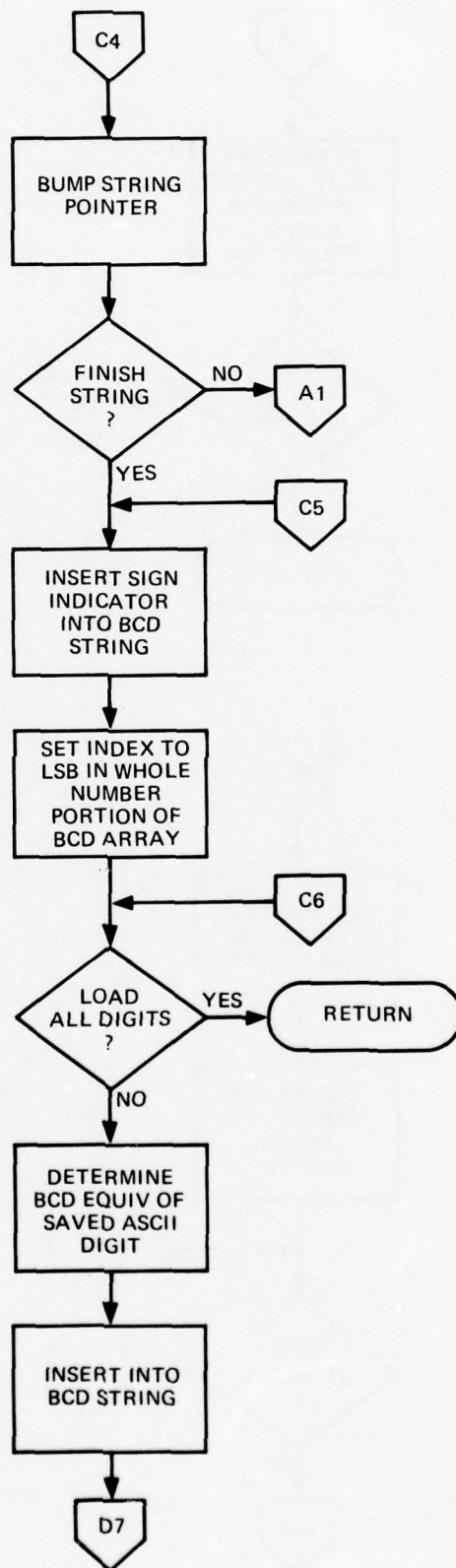
The format of the BCD returned array is shown below.

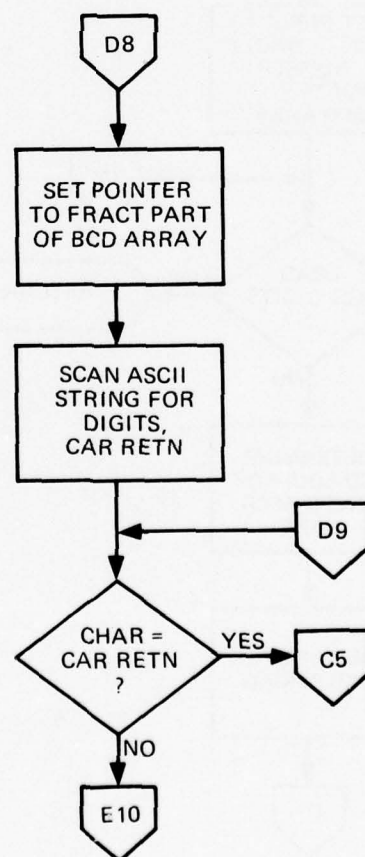
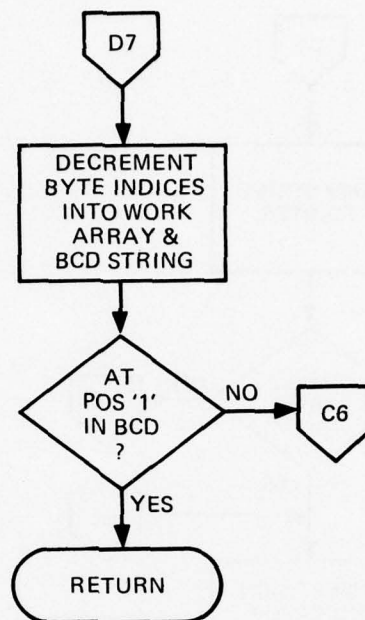
<u>Byte #</u>	<u>Contents</u>
1	Sign (0 = positive, 1 = negative)
2	$10^6$ value
3	$10^5$ value
4	$10^4$ value
5	$10^3$ value
6	$10^2$ value
7	$10^1$ value
8	$10^0$ value
9	$10^{-1}$ value
10	$10^{-2}$ value
11	$10^{-3}$ value
12	Not used

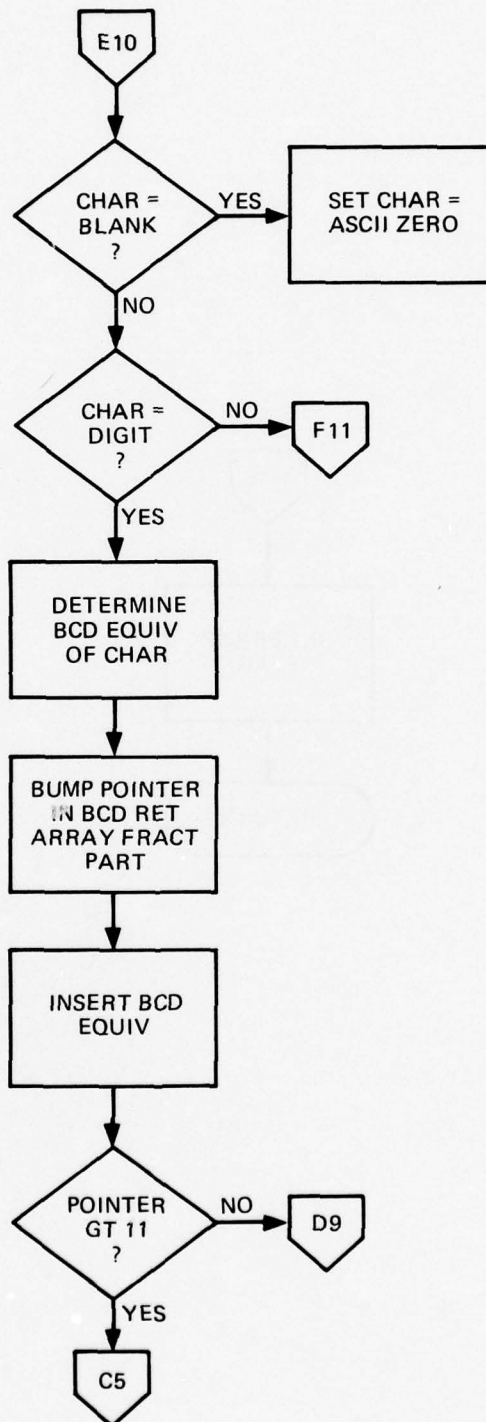


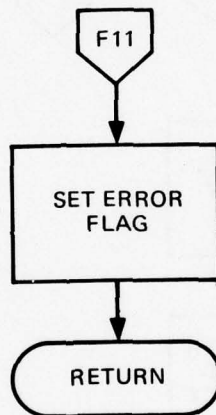














```

C***** SUBROUTINE NUMBER(I,END,IVAL,IERR)*****
C
C**** THE PRIMARY PURPOSE OF THIS ROUTINE IS TO BUILD AN 11 BYTE BCD
C**** ARRAY FROM ASCII INPUT. THE ROUTINE ALSO VERIFIES THAT NO
C**** CHARACTERS OTHER THAN SIGN, DECIMAL POINT, COMMA, OR DIGITS ARE
C**** FOUND IN THE INPUT STRING. THE BEGINNING AND END OF THE STRING
C**** ARE PROVIDED BY THE ISTART AND IEND PARAMETERS.
C**** ZERO RETURNED ARRAY
C
C***** COMMON/IN-OUT/INLINE*****
C***** COMMON/IN-OUT/CHARS,ICAR*****
C***** COMMON/SPECDEC/CHARS,ICAR*****
C***** BYTE INLINE(20),IVAL(12),WORK(20),SIGNA(1)*****
C***** IERR=0*****
C***** DO 10 I=1,12*****
C***** IVAL(I)=2*****
C***** DO 20 I=1,END*****
C***** I=ISTART, IEND*****
C***** CHECK FOR POSITIVE SIGN*****
C***** IF(INLINE(I).EQ.CHARS(3))GO TO 25*****
C***** CHECK FOR NEGATIVE SIGN*****
C***** IF(INLINE(I).EQ.CHARS(4))GO TO 30*****
C***** DO 20 CONTINUE*****
C***** NO SIGN-ASSUME POSITIVE*****
C***** SIGNA(1)=1*****
C***** NUMST=ISTART*****
C***** GO TO 40*****
C***** 25 SIGNA(1)=0*****
C***** NUMST=I+1*****
C***** GO TO 40*****
C***** PUT NEGATIVE SIGN INTO RETURNED ARRAY*****
C***** 30 SIGNA(1)=1*****
C***** NUMST=I+1*****
C***** 40 K=2*****
C***** VERIFY NUMERICS,CAR RETN,COMMAS,OR DECIMAL POINT*****
C***** DO 100 I=NUMST,IEND*****
C***** CHECK CHARACTER IS NUMERIC(CHAR.LE.9.AND.GE.0)*****
C***** IF(INLINE(I).GE.CHARS(1).AND.INLINE(I).LE.CHARS(2))GO TO 90*****
C***** CHECK IF DECIMAL POINT THERE*****
C***** IF(INLINE(I).EQ.CHARS(5))GO TO 200*****
C***** CHECK IF COMMA IN STRING*****
C***** IF(INLINE(I).EQ.CHARS(6))GO TO 100*****
C***** CHECK FOR CAR RETN*****
C***** IF(INLINE(I).EQ.ICAR)GO TO 110*****
C***** IF CHAR NOT A BLANK THAN BAD CHARACTER*****
C***** IF(INLINE(I).NE.CHARS(7))GO TO 300*****
C***** BLANK BECOMES A ZERO*****
C***** INLINE(I)=0*****
C***** SAVE NUMERIC FOUND IN WORK ARRAY*****
C***** K=K+1*****
C***** WORK(K)=INLINE(I)*****
C***** 100 CONTINUE*****

```

```

C**** INSERT THE WHOLE NUMBER PORTION OF THE NUMBER
110 L=0
C**** INSERT SIGN INTO RETURNED ARRAY
      IVAL(1)=SIGNA(1)
120 IF (.EQ.?) RETURN
C**** DETERMINE BINARY VALUE OF ASCII DIGIT
      DO 57 KK=1,10
C**** ASCII DIGITS CONTAINED IN COMMON
      IF (.OR.(KK=1).NE.CHARS(KK+6)) GO TO 57
      KKKK=1
      IVAL(L)=KK
      L=L+1
57 CONTINUE
      KKK=1
      L=L-1
      IF (L.GT.1) GO TO 120
RETURN
C**** INSERT FRACTIONAL PART OF NUMBER IF SPECIFIED
200 L=0
      L=L+1
      IF (L.GT.1) GO TO 110
      DO 250 JJ=1,1END
C**** CHECK FOR CAR RETN
      IF (INLINE(J).EQ.ICAR) GO TO 110
C**** BLANK BECOMES A ZERO
      IF (INLINE(J).EQ.CHARS(7)) INLINE(J)=CHARS(1)
C**** CHECK FOR NON NUMERIC
      IF (INLINE(J).LT.CHARS(1).OR.INLINE(J).GT.CHARS(2)) GO TO 300
C**** DETERMINE BINARY VALUE OF ASCII DIGIT
      DO 223 KK=1,10
      IF (INLINE(J).NE.CHARS(KK+6)) GO TO 223
      KKKK=1
C**** INSERT FRACTIONAL DIGIT
      IVAL(L)=KK
      L=L+1
223 CONTINUE
      IF (L.GT.12) GO TO 110
250 CONTINUE
      GO TO 110
300 CONTINUE
C**** BAD CHARACTER FOUND IN INPUT STRING
      IERR=1
RETURN
END

```

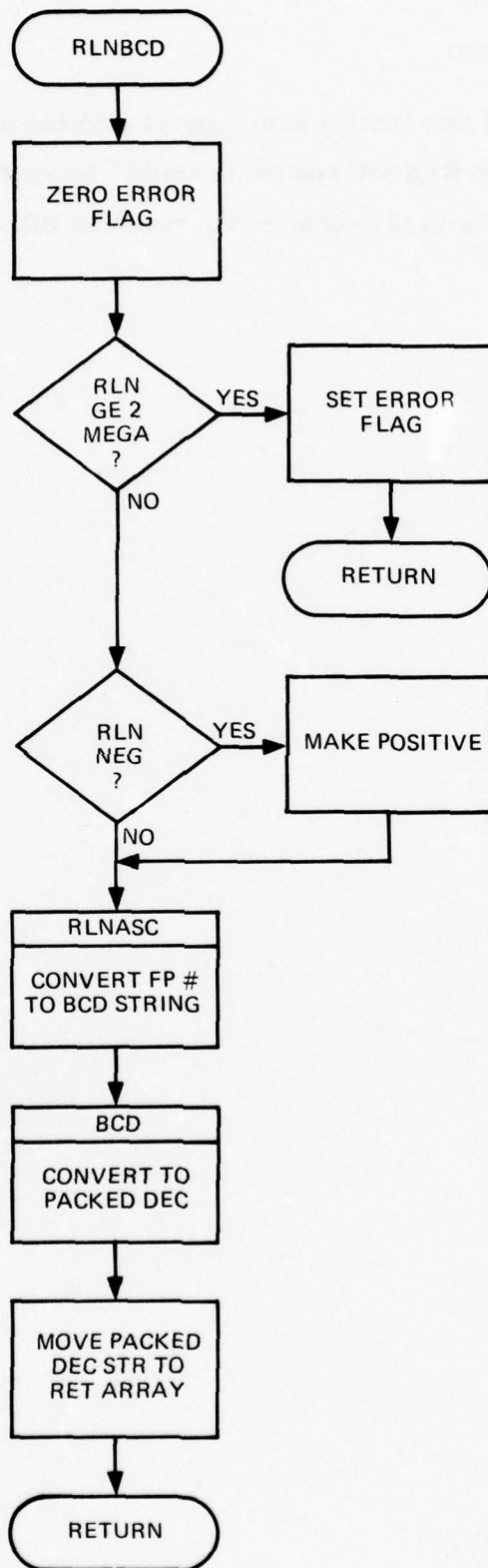
OPTIONS =/ON,/SU,/OP:1

BLOCK	LENGTH
NUMBER 437	(001552)*
INBUF 10	(000020)
SPECDEC 11	(000026)

\*\*COMPILER ----- CODE\*\*  
 PHASE USED FREE  
 DECLARATIVES W0622 W2300  
 EXECUTABLES W0362 W2000  
 ASSEMBLY 01257 W6359

#### SUBROUTINE RLNBCD

The purpose of this routine is to convert a double precision number to packed decimal format. The RLNASC routine is used to convert the number to a BCD string and the BCD routine is used to convert the resultant BCD string to packed decimal.

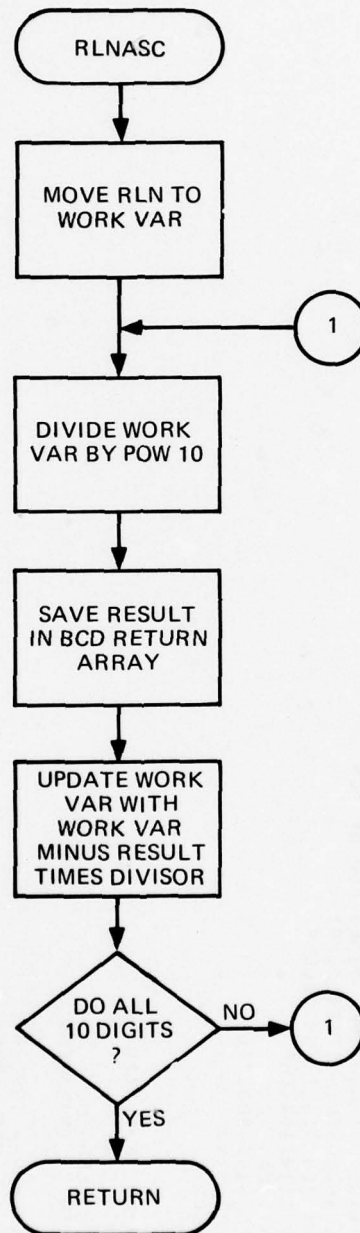






#### SUBROUTINE RLNASC

The purpose of this routine is to convert a double precision number to the BCD representation described in the description of the NUMBER subroutine. The BCD string is generated by a series of divisions of the number by powers of 10 and subtractions of the quotient times the power of 10. Each quotient value, when converted to integer, represents one of the digits of the BCD representation of the number.



```

SUBROUTINE RLNASC(OPRLN,ASCII)
C*****
C***** THE PURPOSE OF THIS ROUTINE IS TO CONVERT A DOUBLE
C***** PRECISION FLOATING POINT NUMBER TO A BCD STRING.
C*****
C*****
C***** DOUBLE PRECISION OPRLN,HOLD,DIVIS(10)
C*****
C***** DATA DIVIS/1.009,1.009,1.007,1.006,1.005,1.004,1.003,
C***** 11.002,1.001,1.002/
C***** HOLD=OPRLN
C***** DO 10 I=1,10
C***** DIVIDE FP NUM BY POWER OF TEN
C***** ITEMP=HOLD/DIVIS(I)
C***** SUBTRACT OUT QUOTIENT TIMES POW OF TEN
C***** HOLD=HOLD-(DIVIS(I)*ITEMP)
C***** SAVE BCD DIGIT FOR CALLER
C***** ASCII(I+1)=ITEMP
C***** 10 CONTINUE
C***** MAKE SIGN POSITIVE
C***** ASCII(1)=A
C***** RETURN
C***** END

```

OPTIONS =/ON,/SU,/OP:1

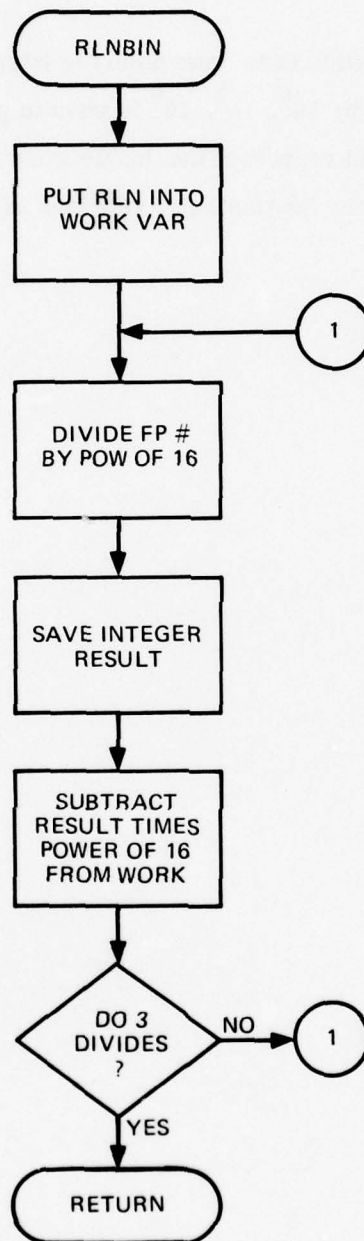
BLOCK LENGTH  
RLNASC 119 (000356)\*

\*\*COMPILER ----- CORE\*\*  
PHASE USED FREE  
DECLARATIVES 00022 02304  
EXECUTABLES 00783 02183  
ASSEMBLY 00965 06601



#### SUBROUTINE RLNBIN

The purpose of this routine is to determine the integer equivalent of a double precision number. Division by  $16^6$ ,  $16^4$ ,  $16^0$  is used to generate integer quotients that if concatenated as bytes would represent the double word integer equivalent of the double precision number. The integer quotients are returned in a 4 element integer array.



```

SUBROUTINE RLNBIN(RLN,BIN)
C*****
C*** THE PURPOSE OF THIS ROUTINE IS TO CONVERT A DOUBLE PRECISION
C*** NUMBER TO BINARY. THE ROUTINE RETURNS A 4 WORD INTEGER ARRAY
C*** WHOSE LOW BYTE VALUES WHEN CONCATENATED TOGETHER WILL GIVE THE
C*** BINARY EQUIVALENT OF THE FP NUMBER.
C
C*****
C*** DOUBLE PRECISION RLN,HOLD
C*** INTEGER H(4)
C*** DOUBLE PRECISION DIVIS(4)
C*** DOUBLE PRECISION HEX
C*** INTEGER ITEMP(2)
C*** BYTE BYT(4)
C*** EQUIVALENCE (BYT(1),ITEMP(1))
C*** PUT FP NUMBER INTO WORK VARIABLE
C*** HOLD=RLN
C*** HEX=16.
C*** J=6
C*** DO 20 I=1,4
C*** GENERATE DIVISOR
C*** DIVIS(I)=HEX**J
C*** DIVIDE TO GENERATE QUOTIENT IN 0-255 RANGE
C*** JTEMP=HOLD/DIVIS(I)
C*** J=J-2
C*** SUBTRACT INTEGER RESULT TIMES DIVISOR
C*** HOLD=HOLD-(JTEMP*DIVIS(I))
C*** SAVE REMAINDER
C*** BIN(I)=JTEMP
C*** 20 CONTINUE
C*** RETURN
C*** END

```

```

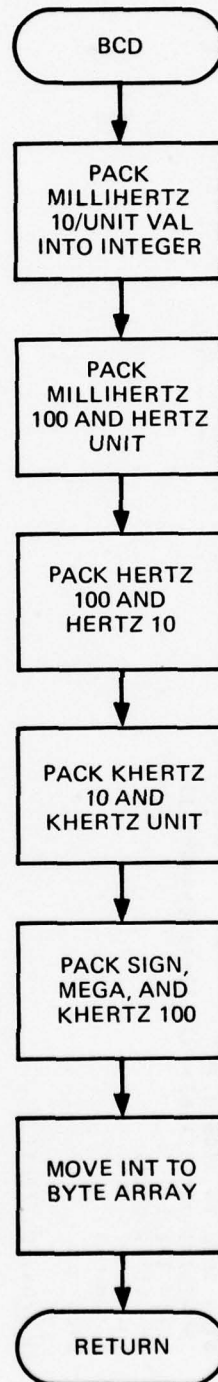
OPTIONS =/ON,/SU,/OP:1
BLOCK LENGTH
RLNBIN 130 (000400)*
**COMPILER ----- CORE**
PHASE USED FREE
DECLARATIVES 00522 02344
EXECUTABLES 00793 02173
ASSEMBLY 01421 06585

```

#### SUBROUTINE BCD

The purpose of this routine is to convert a BCD string to five packed decimal bytes. The format of the BCD string is described with the description of the NUMBER subroutine. A description of the packed decimal form is contained in the real-time mode section.





OPTIONS = /ON, /S, /OP

BLOCK	LENGTH
B00	154 (000464)*

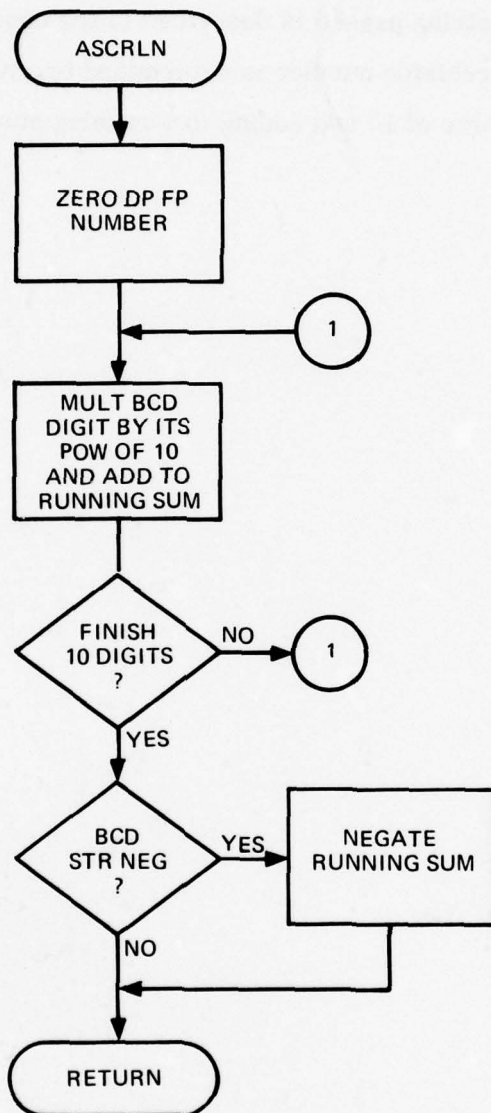
```

**COMPILER ----- CODE**
      PHASE      USED   FREE
DECLARATIVES 00622 02344
EXECUTABLES  00563 02103
ASSEMBLY      00977 06629

```

#### SUBROUTINE ASCRLN

The purpose of this routine is to perform BCD to double precision conversion. The format of the BCD string passed is described in the description of the NUMBER subroutine. A double precision number is determined by multiplying each BCD digit by its corresponding power of 10 and adding to a running sum.





```

SUBROUTINE ASCRLN(ASCII,KLN)
C*****
C**** THE PURPOSE OF THIS ROUTINE IS TO CONVERT AN BCD
C**** NUMERIC STRING TO A FLOATING POINT DOUBLE PRECISION
C**** NUMBER. SUCCESSIVE MULTIPLICATIONS BY THE APPROPRIATE
C**** POWER OF TEN AND ADDITIONS TO A RUNNING SUM WILL
C**** YIELD THE DESIRED FLOATING POINT NUMBER.
C*****
C***** DOUBLE PRECISION RMULT(10),KLN
C***** BYTE ASCII(12)
C***** DATA RMULT/1.009,1.008,1.007,1.006,1.005,1.004,1.003,
C***** 1.002,1.001,1.000/
C**** ZERO FLOATING POINT RESULT
KLN=0.
DO 10 I=1,10
C**** ADD TO SUM BCD DIGIT TIMES ITS POWER OF TEN
KLN=KLN+(RMULT(I)*ASCII(I+1))
10 CONTINUE
C**** CHECK IF BCD STRING IS NEGATIVE
J=ASCII(1)
IF (J.EQ.1) KLN=-KLN
RETURN
END

```

OPTIONS =/ON,/SU,/OP:1

BLOCK LENGTH  
ASCRLN 131 (000006)\*

\*\*COMPILER ----- CODE\*\*  
PHASE USED FREE  
DECLARATIVES 00622 02344  
EXECUTABLES 00783 02183  
ASSEMBLY 00989 06617

## REAL-TIME MODULE

The real-time module is responsible for loading the main program and reader routine into RAM, performing the system parameter and pattern value table input from PDP-11, and executing the real-time mode. The module is composed of a main program that executes the real-time mode, a reader program that performs the input from the PDP-11, and a loader program to load the main and reader programs.

Detailed descriptions of each program follow.

## REAL-TIME MAIN

This program is designed to output a random frequency to the Rockland synthesizer in real-time. A cycle rate of approximately 2.45 milliseconds has been obtained and is maintained in software by delay loops when necessary. Since no internal hardware clock accessible to software is present in the Inteltec, this is the only feasible method of maintaining a fairly uniform cycle rate.

The system parameter tables and pattern value tables for the HOP, MFSK, and Doppler effects are obtained from the PDP-11 via a down line load process using the DL11 interface and Inteltec serial input/outputs. The format of the system parameter table is shown in Figure 8.

In order to simulate current time, the program maintains a counter that is updated after each output to the Rockland frequency synthesizer. This counter is initialized to zero at the start of the real-time run. There are also three counters for each of the three effect types that are initialized in static mode and updated by their cycle rate each time a corresponding effect pattern value is used in computing an output frequency for the Rockland. During each cycle, all three effect counters are compared with the value of the simulation counter. If the effect counter value is less than or equal to the simulation counter value, then a value for that effect is used in computing the Rockland frequency. When no effect types satisfy this requirement, only the base frequency is output.

Both the base frequency and pattern value tables are stored in packed decimal form. The format of this storage is given in Figure 9. A running sum, also in packed decimal form, is initialized at the beginning of each cycle period to that of the base frequency. Effect values are added or subtracted from the current running sum value using BCD arithmetic. The addition and subtraction routines used have been programmed using straightline repetitive code to minimize the time required for these time consuming operations. A delay loop is used with the addition routine to account for the longer time required for the subtraction process.

ADR		TYPE	LENGTH
20	SIMULATION CURRENT CYCLE	BINARY	3
23	BASE FREQUENCY	PACKED DEC	5
28	RUNNING SUM	PACKED DEC	5
2D	SIMULATION STOP VALUE	BINARY	3
30	HOP CURRENT CYCLE	BINARY	3
33	RANDOM NUMBER INDICATOR (FF)	BINARY	1
34	HOP RANDOM NUMBER MASK	BINARY	1
35	HOP RANDOM NUMBER SEED	BINARY	3
38	HOP PATTERN TABLE LOC	BINARY	2
3A	HOP CYCLE RATE	BINARY	2
3C	HOP STOP VALUE	BINARY	3
3F	MFSK CURRENT CYCLE	BINARY	3
42	RANDOM NUMBER INDICATOR (FF)	BINARY	1
43	MFSK RANDOM NUMBER MASK	BINARY	1
44	MFSK RANDOM NUMBER SEED	BINARY	3
47	MFSK PATTERN TABLE LOC	BINARY	2
49	MFSK CYCLE RATE	BINARY	2
4B	MFSK STOP VALUE	BINARY	3
4E	DOP CURRENT CYCLE	BINARY	3
52	DOP TABLE INDEX	BINARY	2
55	NOT USED		
58	DOP PATTERN TABLE LOC	BINARY	2
5A	DOP CYCLE RATE	BINARY	2
5C	DOP STOP VALUE	BINARY	3

\*All fields are in LSB to MSB order

Figure 8. System Parameter Table



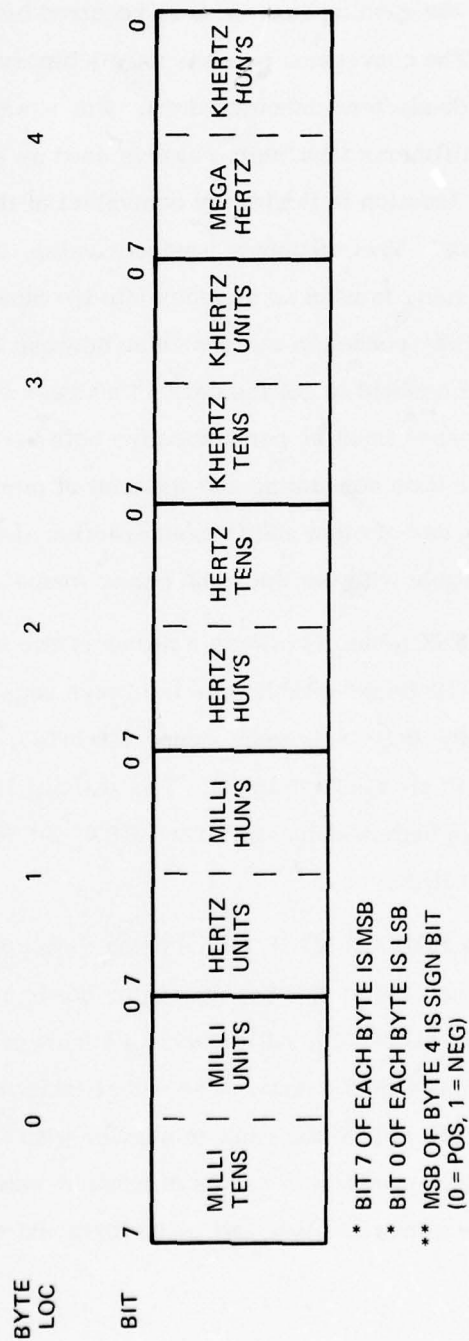


Figure 9. Pattern Storage Format

Since the output format required by the Rockland, see Figure 10, is binary, not packed decimal, a conversion of the running sum value is required before output to the synthesizer can be performed. The conversion process uses a binary equivalent table in tens/units, hundreds, and hundreds/tens denominations. For example, byte one of the running sum containing the millihertz tens/units value is used as an index into the tens/units tables. Stored at this location is the binary equivalent of the tens/units packed decimal value specified in byte one. The millihertz hundreds value, stored in the lower nibble of byte two of the running sum, is used as an index into the hundreds equivalent table. Since two bytes are generally needed to store a value between 0 and 900, the millihertz hundreds digit must be doubled to get the correct address of the two byte binary equivalent. Similar processes must be performed for both hertz and kilohertz. The conversion process, although time consuming and wasteful of memory, has been found to be more economical than use of other addition/subtraction algorithms that generate a running sum more compatible with the Rockland output format.

The size of the HOP and MFSK tables is always a power of two up to a maximum of 128 for HOP and 64 for MFSK. The Doppler table size is always equal to 1024. Allowing for a fixed five bytes per value, the HOP table may occupy 640 bytes, the MFSK table 320 bytes, and the Doppler table is always 5120 bytes. The starting location for each table is not variable. HOP always begins at location 1A00 HEX, MFSK at location 1000 HEX, and Doppler at location 600 HEX.

Values are chosen from the HOP and MFSK tables using a pseudorandom number generator for index selection. The random number generator used, a P-N sequence based on a primitive polynomial of degree 24, will provide a series of three byte random numbers that will not repeat for more than 1 hour. The actual table index chosen is gotten by a masking operation on the LSB of the random number with a mask value one less than table size. This technique produces a series of random numbers whose values will range from zero to table size minus one that will be uniform and will repeat each index with equal probability.

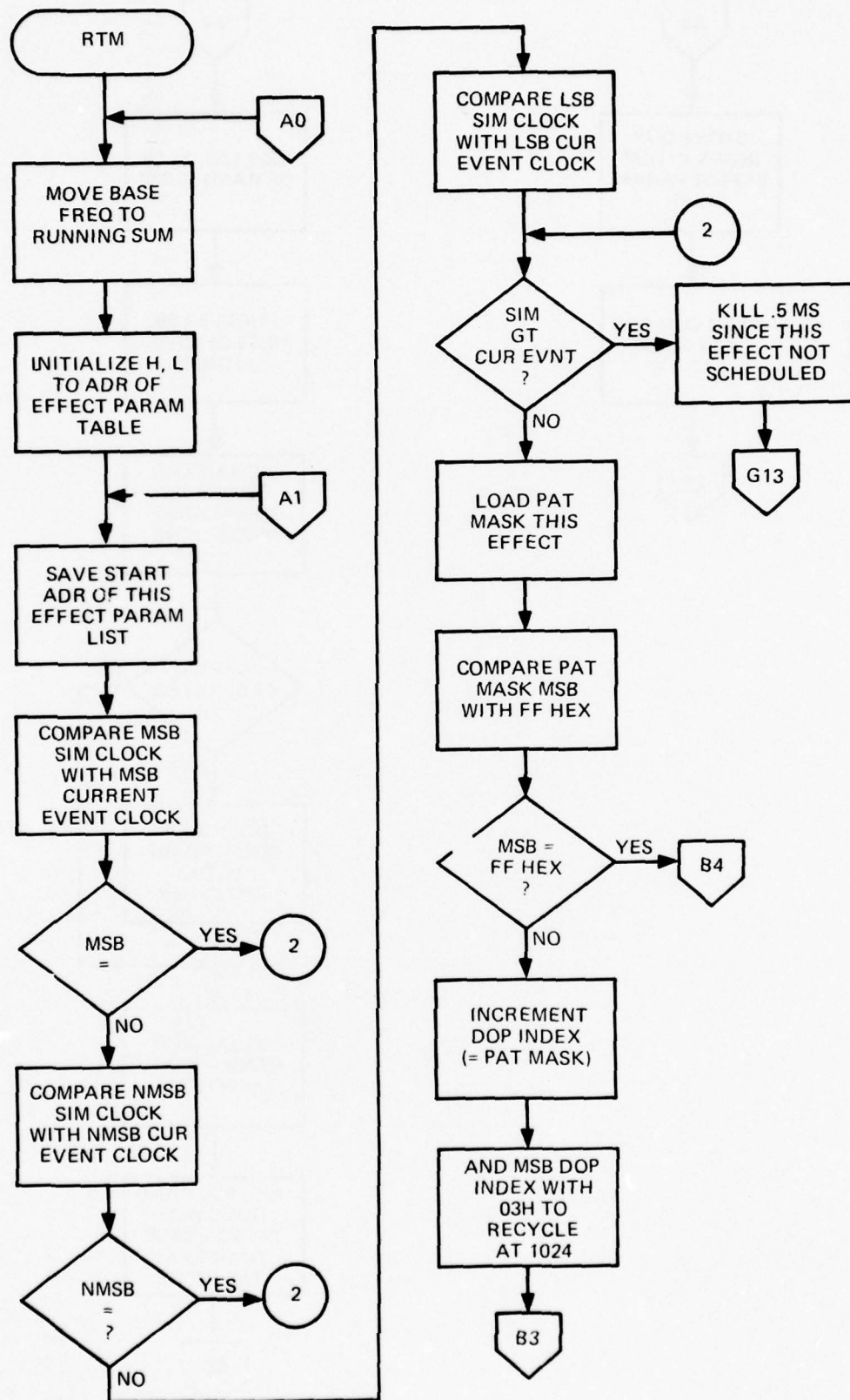
	PORT #
MILLIHERTZ LSB (BINARY)	8
MILLIHERTZ MSB (BINARY)	9
HERTZ LSB (BINARY)	10
HERTZ MSB (BINARY)	11
KILOHERTZ LSB (BINARY)	12
KILOHERTZ MSB (BINARY)	13
MEGAHERTZ	14

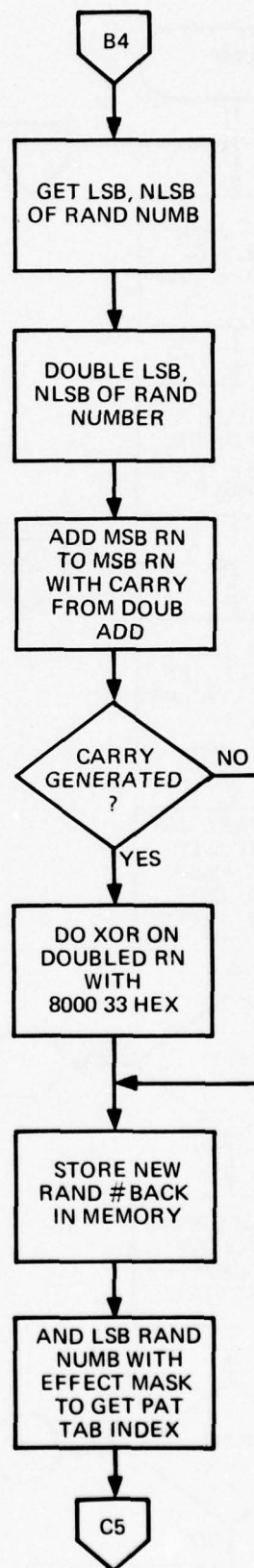
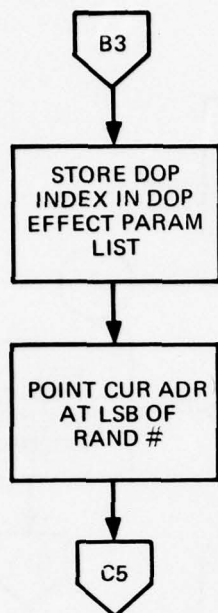
\*\*Binary value of 0 output followed by binary value of 1, both to  
PORT 15 signals output

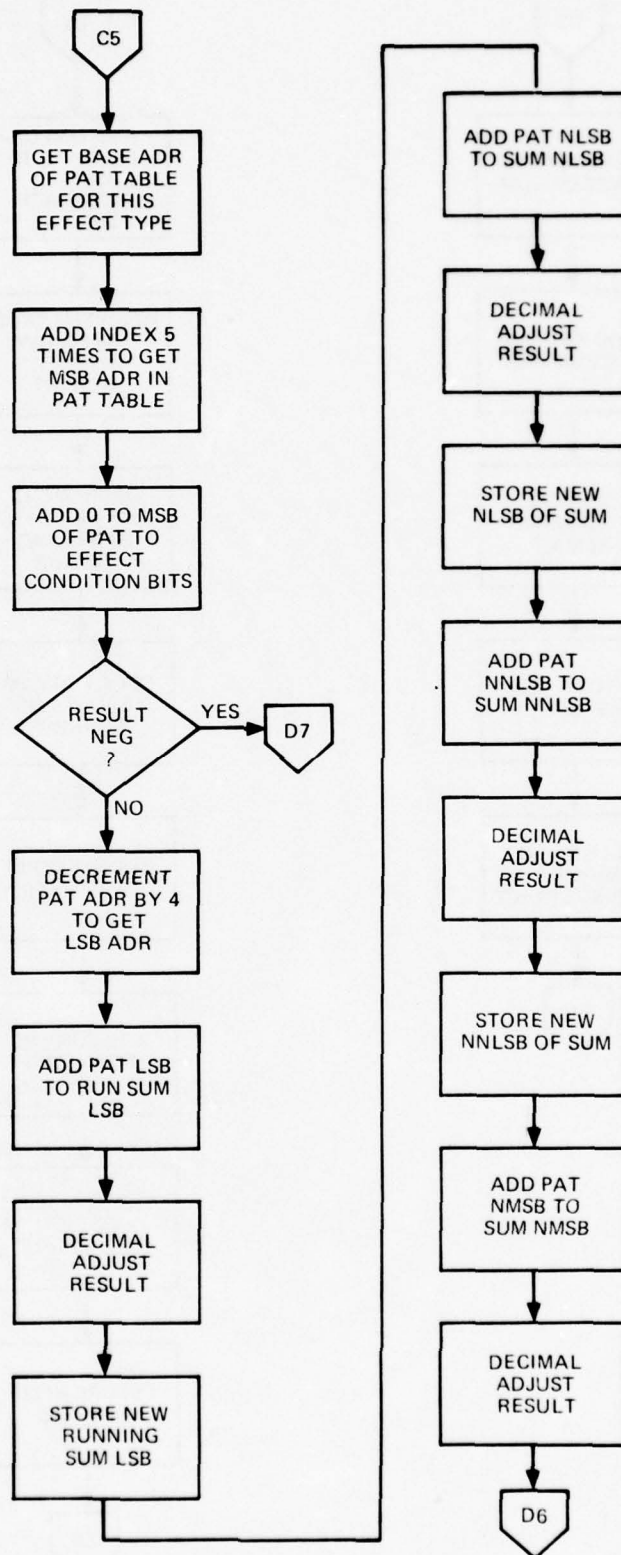
Figure 10. Rockland Interface Format

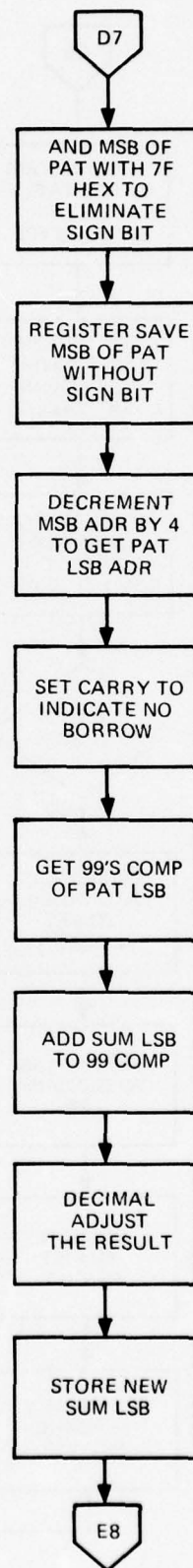
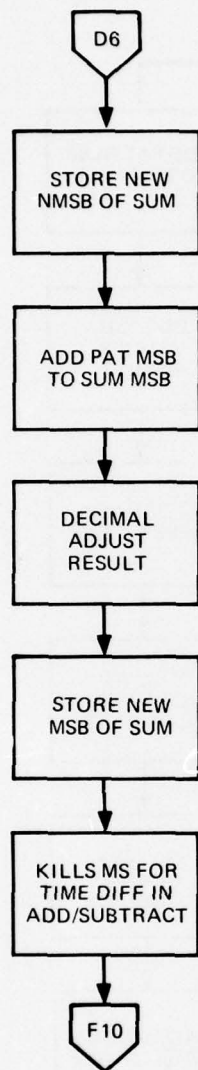
Values are chosen from the Doppler table using an index value that is merely incremented after each selection. When the index value exceeds table size, the index is reset to zero to begin another Doppler cycle.



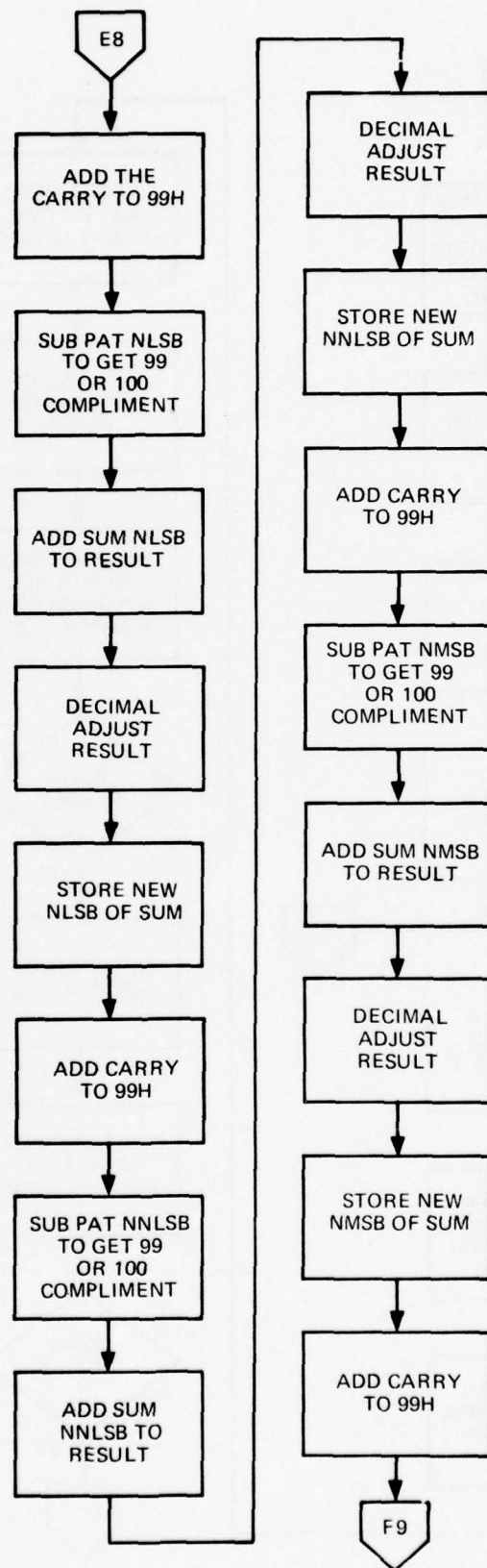


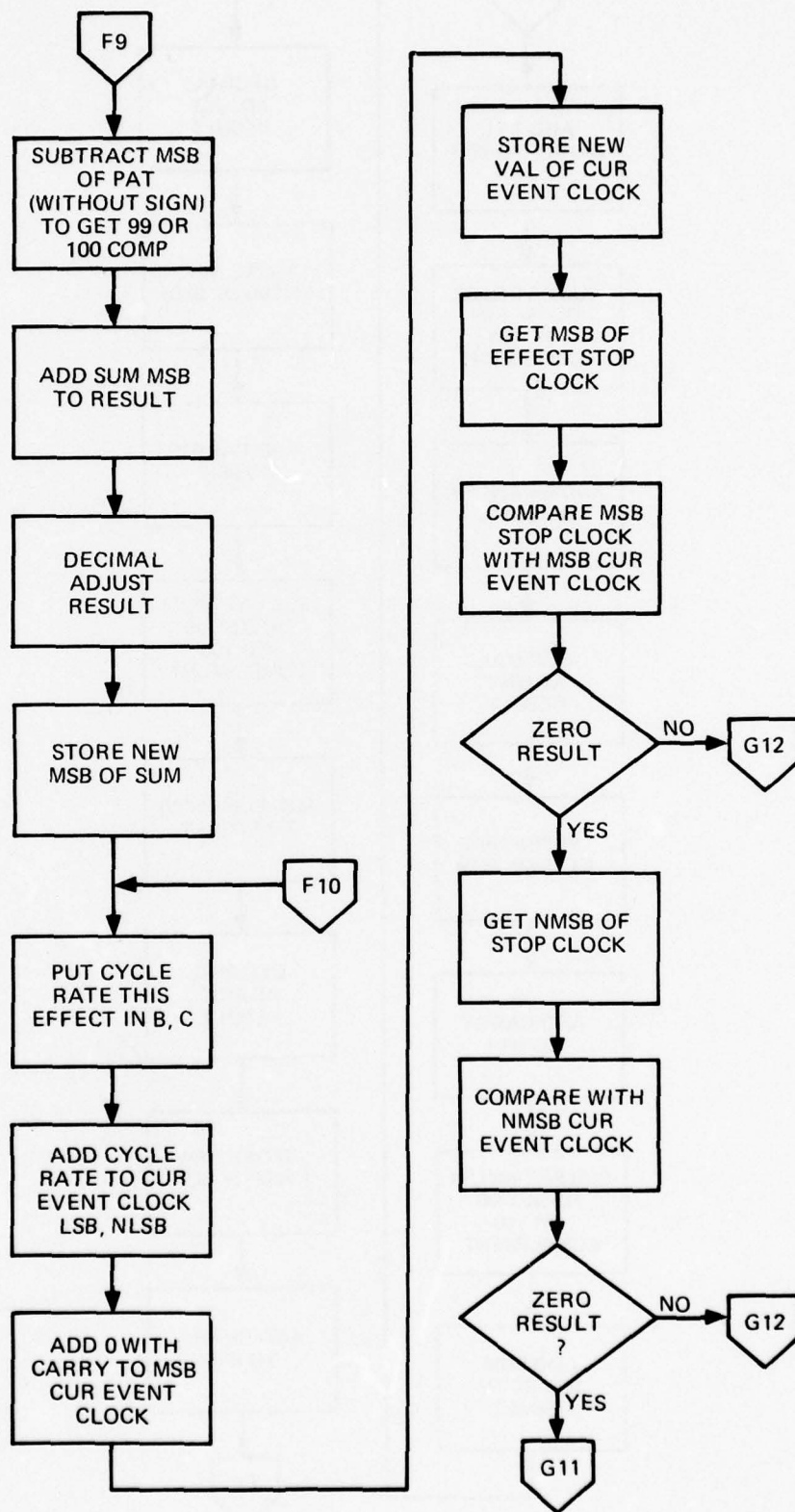


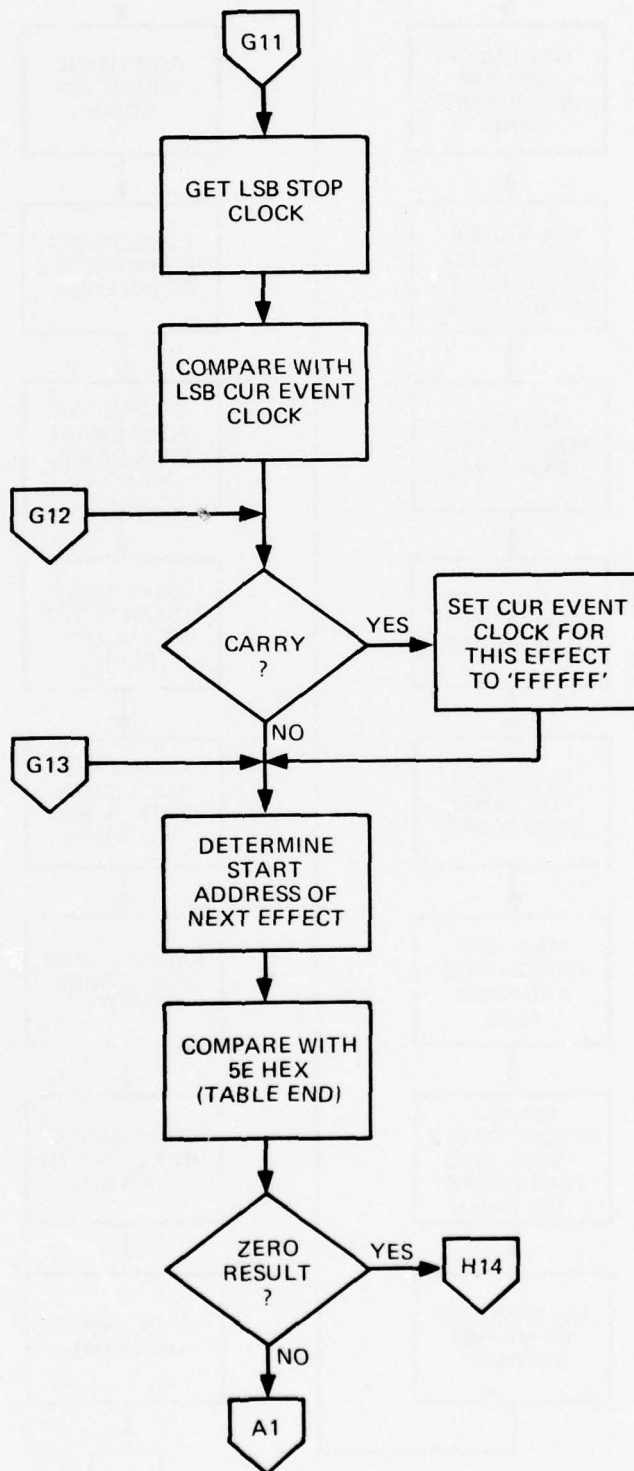


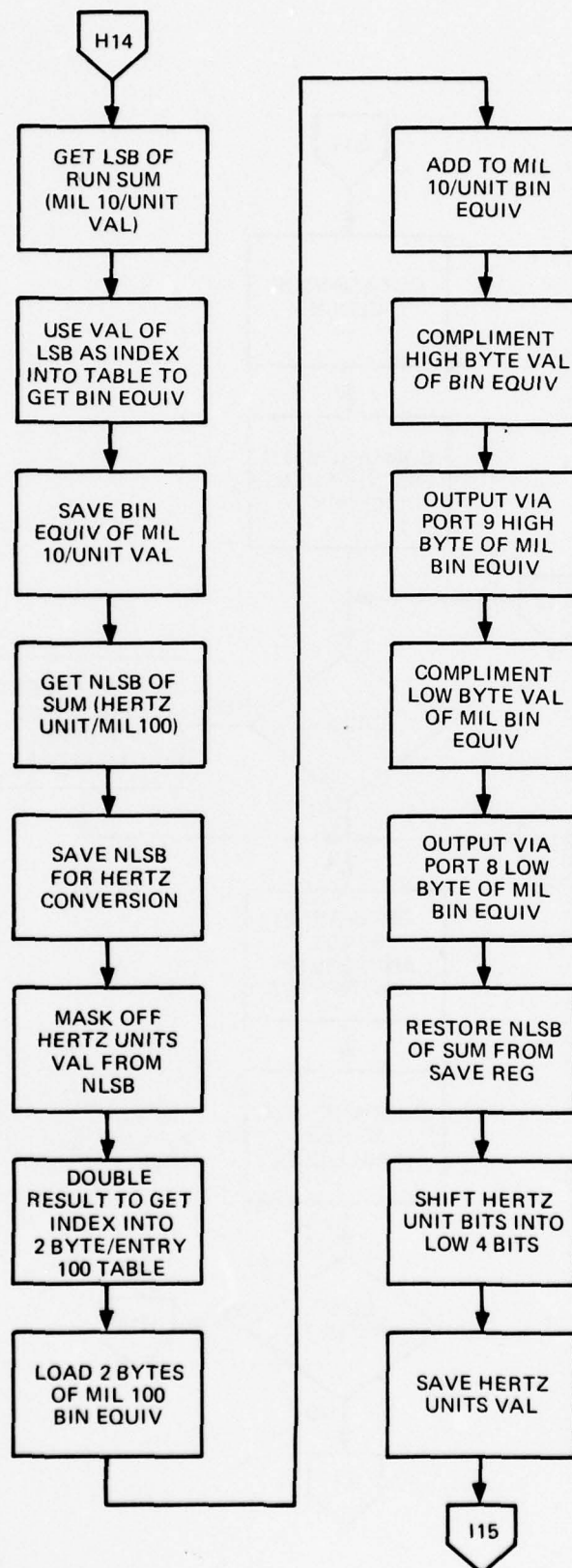




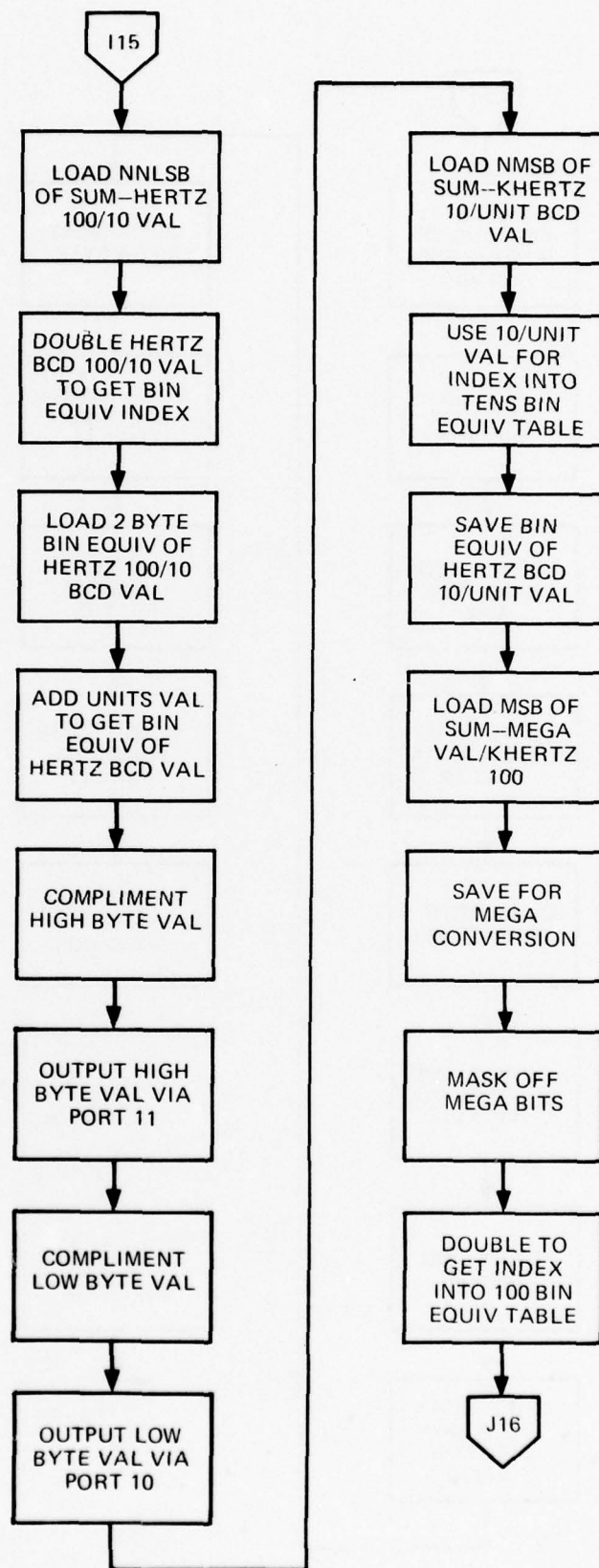


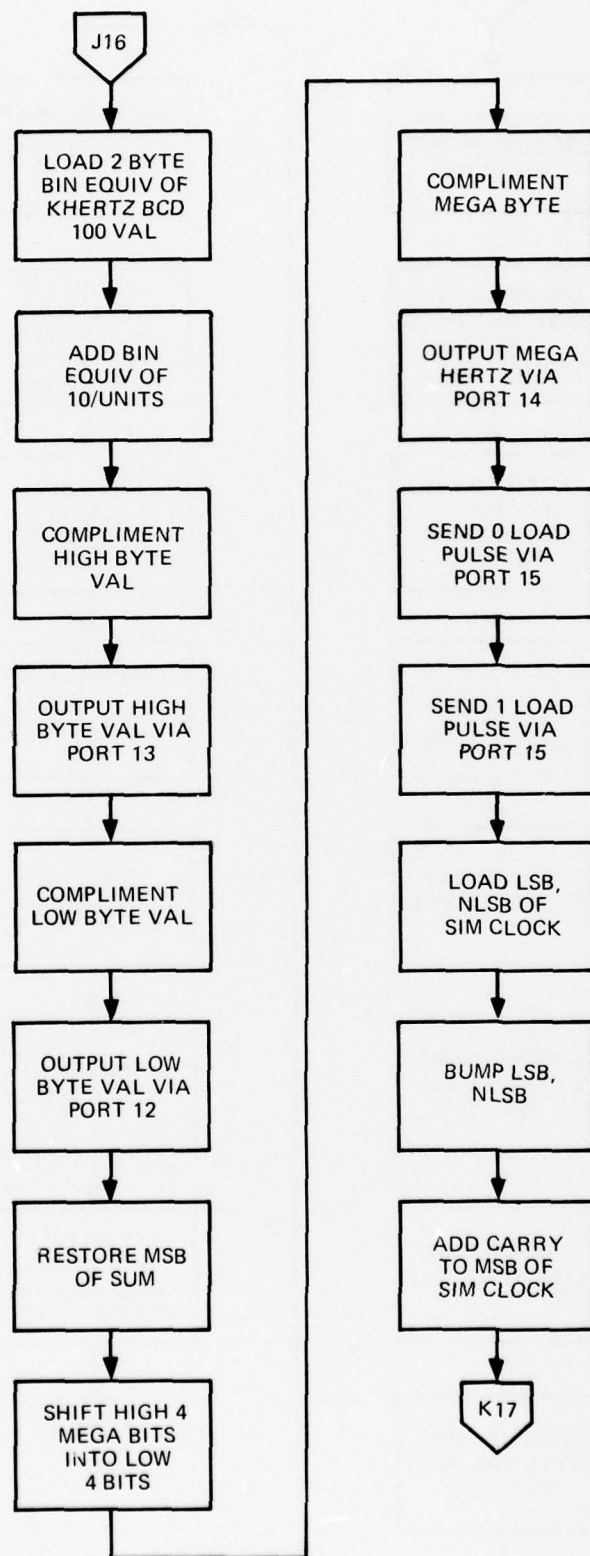


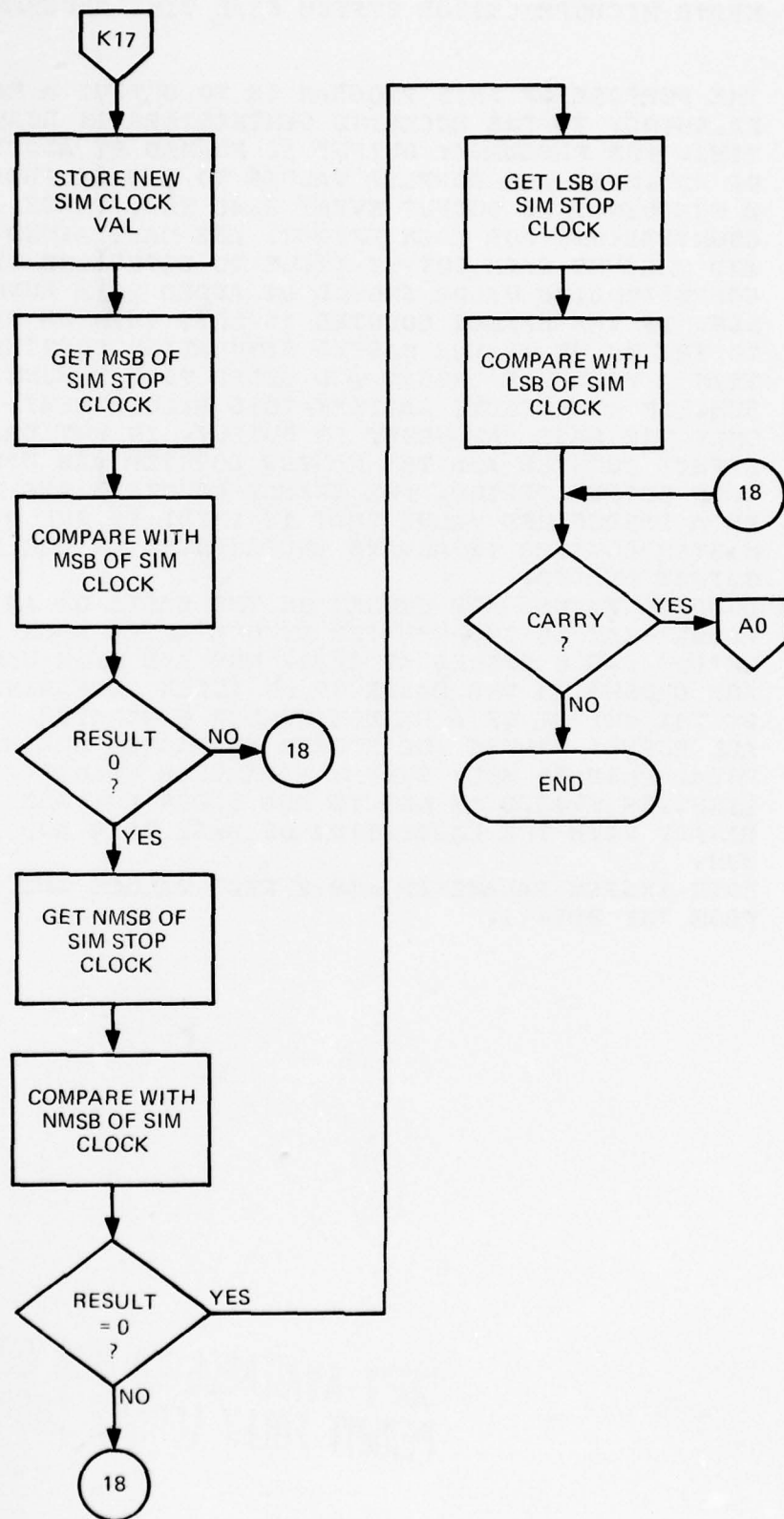












```

***** KBAND MICROPROCESSOR SYSSYM REAL TIME PROGRAM
;
;
; THE PURPOSE OF THIS PROGRAM IS TO OUTPUT A RANDOM
; FREQUENCY TO THE ROCKLAND SYNTHESIZER IN REAL
; TIME. THE FREQUENCY OUTPUT IS FORMED BY ADDITION
; OF HOP,MFSK,AND DOPPLER VALUES TO A BASE FREQ.
; A FREQUENCY IS OUTPUT EVERY 2.45 MLS. THREE
; COUNTERS(ONE FOR EACH EFFECT) ARE MAINTAINED
; AND CHECKED EACH OUTPUT CYCLE TO DETERMINE IF ITS
; CORRESPONDING VALUE SHOULD BE ADDED TO A RUNNING
; SUM. IF THE EFFECT COUNTER IS LESS THAN OR EQUAL
; TO THE VALUE OF THE MASTER SIMULATION COUNTER
; THAN A VALUE IS CHOSEN AND ADDED TO THE RUNNING
; SUM. IF NO EFFECTS SATISFY THIS REQUIREMENT, THAN
; ONLY THE BASE FREQUENCY IS OUTPUT. IN ANY CASE EA
; EFFECT COUNTER AND THE MASTER COUNTER ARE UPDATED
; EACH OUTPUT PERIOD. THE EFFECT COUNTERS ARE UPDAT
; BY A PREDEFINED VALUE THAT IS INPUT BY THE USER.
; MASTER COUNTER IS ALWAYS INCREMENTED BY ONE EACH
; OUTPUT PERIOD.
; DOPPLER VALUES ARE CHOSEN ON THE BASIS OF AN INDE
; VALUE THAT IS INCREMENTED BY ONE AFTER EACH SEL-
; ECTION AND RECYCLED AT 1024. HOP AND MFSK VALUES
; ARE CHOSEN ON THE BASIS OF AN INDEX DETERMINED
; BY THE OUTPUT OF A RANDOM NUMBER GENERATOR.
; ALL EFFECT VALUES ARE STORED IN PACKED DECIMAL
; FORM, NLSB TO MSB. SYSTEM PARAMETER VALUES ARE
; LIKEWISE STORED IN LSB TO MSB ORDER BUT ARE ALL I
; BINARY WITH THE EXECEPTION OF BASE FREQ AND RUNNI
; SUM.
; BOTH SYSTEM PARAMETER AND EFFECT VALUES ARE INPUT
; FROM THE PDP-11.

```

COPY AVAILABLE TO DDC DOES NOT  
PERMIT FULLY LEGIBLE PRODUCTION



COPY AVAILABLE TO DDC DOES NOT  
PERMIT FULLY LEGIBLE PRODUCTION

\*\*\*\*\* SYSTEM TABLES-DATA AREA DEFINITIONS

```

;
0000      ORG      20H
0020      SIM:    DS      3      ;SIMULATION CLOCK
0023      BFREQ:  DS      5      ;BASE FREQ
0028      SFREQ:  DS      5      ;RUNNING SUM
002D      STOP:   DS      3      ;STOP CLOCK FOR SIMULATION
;
;
SYSTB:
0030      DS      3      ;HOP CUR EVENT CLOCK
0033      DS      2      ;HOP PATTERN MASK
0035      DS      3      ;HOP RAND NUMB SEED
0038      DS      2      ;HOP PAT ADR(1A00)
003A      DS      2      ;HOP CYCLE RATE
003C      DS      3      ;HOP STOP TIME
;
003F      DS      3      ;MFSK CUR EVENT CLOCK
0042      DS      2      ;MFSK PAT MASK
0044      DS      3      ;MFSK RAND NUMB SEED
0047      DS      2      ;MFSK PAT ADR(1D00)
0049      DS      2      ;MFSK CYCLE RATE
004B      DS      3      ;MFSK STOP TIME
;
004E      DS      3      ;DOP CUR EVENT CLOCK
0051      DS      2      ;DOP PAT INDEX
0053      DS      3      ;NOT USED FOR DOP
0056      DS      2      ;DOP PAT LOCATION(600)
0058      DS      2      ;DOP CYCLE RATE
005A      DS      3      ;DOP STOP TIME
005D      ENDD:   DS      1
005E      SAV:    DS      2
0063      TEN     EQU     03      ;HIGH BYTE ADR OF 10/UNIT BIN TAB
0064      HUN     EQU     04      ;HIGH BYTE ADR OF 100/10 BIN TABL
;
;
***** ESTABLISH RUNNING SUM-SETUP ADDRESSES ETC
;
0060 012300  STEP3: LXI      D,BFREQ ;LOAD ADR OF BASE FREQ
0063 210000  LXI      H,SFREQ ;LOAD ADR OF RUNNING SUM
0066 1004    HVI      D,4
0068 0A      HVE:   LOAX    B
0069 77      MOV     H,A      ;MOVE BASE BYTE TO SUM
006A 0C      INR     C      ;ADR NEXT RAND BYTE
006B 2C      INR     L      ;ADR NEXT SUM BYTE
006C 15      DCR     D
006D F26300  JP      HVE      ;MOVE ANOTHER BYTE
0070 210000  LXI      H,SYSTB ;START ADR OF SYS TABLE

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)
)**** DETERMINE IF THIS EFFECT WILL BE INCLUDED
)
0073 5A STEP1: MOV D,H
0074 5D MOV E,L
0075 225E00 SHLD SAV )SAVE START ADR OF THIS EFFECT
0078 2C INR L )ADR MSB CUR EVENT
0079 2C INR L )ADR MSB CUR EVENT
007A 012200 LXI B,SIM+2 )ADR MSB OF SIM CLOCK
007D 0A LDAX B )LOAD MSB SIM CLOCK
007E EE CMP M )COMPARE WITH MSB CUR EVENT CLOCK
007F C28D00 JNZ CTME
0082 0D DCR C )ADR MSB SIM CLOCK
0083 2D DCR L )ADR MSB CUR CLOCK
0084 0A LDAX B )LOAD MSB SIM CLOCK
0085 EE CMP M )COMPARE WITH MSB CUR EVENT CLOC
0086 C28D00 JNZ CTME
0089 0D DCR C )ADR LSB OF SIM CLOCK
008A 2D DCR L )ADR LSB CUR EVENT CLOCK
008B 0A LDAX B )LOAD LSB SIM CLOCK
008C EE CMP M )COMPARE WITH LSB CUR EVENT CLOCK
008D D29900 CTME: JNC STEP2 )NO CAR-SIM GT = CUR EVENT
)
)**** THIS EFFECT NOT INCLUDED-KILL TIME TAKEN IF EFFEC
)**** WAS INCLUDED
)
0090 3E3C MVI A,60
0092 3D NO: DCR A
0093 F29200 JP NO
0096 C3A901 JMP OK )NOW CHECK IF THIS WAS LAST EFFEC
)
)**** DETERMINE IF DOPPLER EFFECT-IF YES GET DOPPLER IN
)**** OTHERWISE GO GENERATE RANDOM # FOR INDEX VAL
)
0099 EB STEP2: XCHG )START THIS EFFECT WAS IN D,E
009A 2C INR L )ADR MSB CUR EVENT
009B 2C INR L )ADR MSB CUR EVENT
009C 2C INR L )ADR LSB PAT MASK
009D 4E MOV C,M )LOAD LSB PAT MASK
009E 2C INR L )ADR MSB PAT MASK
009F 4E MOV B,M )LOAD MSB PAT MASK
00A0 78 MOV A,B
00A1 EFFF XRI 07FH )CHECK FOR DOP EFFECT-NOT FFH
00A2 C8E200 JZ STEP3 )NOT FFH THEN GET RANDOM # INDEX
)
)**** GET DOPPLER INDEX AND UPDATE
00A6 03 INX B )INCR DOP INDEX
00A7 78 MOV A,B
00A8 E603 ANI 03H )RECYCLE DOP WHEN IT HITS 0024
00A9 77 MOV B,A )STORE NEW MSB DOP INDEX
00AB 2D DCR L )ADR LSB DOP INDEX
00AC 71 MOV L,C )STORE LSB DOP INDEX
00AD 2C INR L )ADR MSB OF DOP IND
00AE 2C INR L )ADR OF LSB OF SEED
00AF C8E200 JZ STEP3 )NOT FFH THEN GET RANDOM # GEN

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```

)
)**** RANDOM # INDEX GENERATION FOR HOP AND MFSK
)
STEP3: INR      L      )ADR OF LSB OF SEED
        MOV      E,M    )LOAD SEED LSB
        INR      L      )ADR NLSB SEED
        MOV      D,M    )LOAD NLSB OF SEED
        INR      L      )ADR MSB OF SEED
        MOV      A,M
        XCHG
        DAD      H      )DOUBLE LSB AND NLSB
        ADC      A      )DOUBLE MSB WITH CARRY FROM DAD
        XCHG
        JNC      STORE  )NO CARRY THEN NO XOR NEEDED
        XRI      8CH    )MSB XOR
        MOV      B,A    )SAVE MSB IN B
        XRA      A      )NLSB MASK=0
        XRA      D      )NLSB XOR
        MOV      D,A    )SAVE NLSB IN D
        MVI      A,33H  )LSB MASK
        XRA      E      )LSB XOR
        MOV      E,A    )SAVE LSB IN E
        MOV      A,B    )MSB BACK TO A
)
)**** STORE OFF NEW RANDOM NUMBER
)
STORE: MOV      M,A    )SAVE MSB
        DCR      L
        MOV      H,D    )NEW NMSB
        DCR      L
        MOV      M,E    )NEW LSB
)
)**** GET INDEX FROM LSB OF RANDOM # USING MASK FROM TH
)
        MOV      A,E    )LSB STILL IN E
        XRA      C      )MASK WAS IN C FROM STEP 2
        MOV      C,A    )SETUP B,C WITH INDEX
        XRA      A      )HIGH INDEX VAL IS ZERO
        MOV      B,A
)
)**** GET BYTE LOC OF FREE BY MULT OF INDEX BY 5 AND AD
)**** TO THE BASE ADDRESS OF THE PARTICULAR PATTERN TABL
)
STEP4: INR      L      )ADR OF NLSB OF SEED
        INR      L      )ADR OF MSB OF SEED
        INR      L      )ADR OF LSB PAT LOC
        MOV      E,M    )LSB OF PAT BASE ADR
        INR      L      )ADR OF MSB OF ADR
        MOV      D,M    )MSB OF PAT BASE ADR
        XCHG
        DAD      B      )BASE ADR TO H,L-OUR ADR TO D,E
        DAD      B      )ADD INDEX 5 TIMES TO GET ACT ADR
        DAD      B
        DAD      B
        DAD      B
        DAD      B      )ADR OF FREE NOW IN H,L

```



```

***** BCD ADDITION ROUTINE-SUM+PATTERN
;
00EC C30001      JMP      CONT      ;JUMP OVER MONITOR STACK AREA(F0-
00E3             ORG        100H

CONT:
0100 1E20      MVI      E,SFREQ ;ADR OF RUNNING SUM
0102 7E        MOV      A,M      ;LOAD MSB OF PATTERN
0103 C600      ADI      0        ;AFFECT SIGN CONDITION
0105 FA3101     JM       DSUB     ;SIGN BIT SET-HAVE NEG FREQ
0103 2B        DCX      H        ;GET LSB OF PATTERN
0109 2B        DCX      H
010A 2B        DCX      H
010B 2B        DCX      H

***** ADDITION OF LSB BYTES
010C 1A        LDAX     D        ;LOAD LSB OF SUM
010D 8E        ADC      M        ;ADD LSB OF PAT TO IT
010E 27        DAA       ;BCD ADJUST
010F 12        STAX     D        ;STORE NEW LSB OF SUM

***** NLSB ADDITION
0110 13        INX      D        ;ADR OF NLSB OF SUM
0111 23        INX      H        ;ADR NLSB OF PAT
0112 1A        LDAX     D        ;LOAD NLSB OF SUM
0113 8E        ADC      M        ;ADD TO IT PAT NLSB
0114 27        DAA       ;BCD ADJUST
0115 12        STAX     D        ;STORE NEW NLSB OF SUM

***** NNLSB ADDITION
0116 13        INX      D        ;ADR NNLSB BYTE
0117 23        INX      H        ;ADR NNLSB OF PAT
0118 1A        LDAX     D        ;LOAD NNLSB
0119 8E        ADC      M        ;ADD IN NNLSB OF PAT
011A 27        DAA       ;BCD ADJUST
011B 12        STAX     D        ;STORE NEW NNLSB OF SUM

***** NNNLSB ADDITION
011C 13        INX      D        ;ADR OF NNNLSB OF SUM
011D 23        INX      H        ;ADR OF NNNLSB OF PAT
011E 1A        LDAX     D        ;LOAD NNNLSB OF SUM
011F 8E        ADC      M        ;ADD TO PAT
0120 27        DAA       ;BCD ADJUST
0121 12        STAX     D        ;STORE NEW NNNLSB OF SUM

***** MSB ADDITION
0122 13        INX      D        ;ADR OF SUM BYTE
0123 23        INX      H        ;ADR OF PAT BYTE
0124 1A        LDAX     D        ;LOAD SUM BYTE
0125 8E        ADC      M        ;ADD TO PAT
0126 27        DAA       ;BCD ADJUST
0127 12        STAX     D        ;NEW MSB OF SUM

;
***** KILL TIME FOR DIFFERENCE IN AD SUB ROUTINES
;
0128 3E06      MVI      A,6
012A 3D        DCR      A
012B F22A01     JP       5-1
012E C37001     JMP      STEPS

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)
)**** BCD SUBTRACTION ROUTINE
)
DSUB:
0131 E67F      ANI      07FH      )GET RID OF SIGN BIT FROM PAT
0133 4F        MOV      C,A      )SAVE MSB OF PAT
0134 2B        DCX      H        )GET ADR OF LSB OF PAT
0135 2B        DCX      H
0136 2B        DCX      H
0137 2B        DCX      H        )LSB ADR IN H,L
)**** LSB SUBTRACTION
0138 6699      MVI      B,99H    )USED IN GETTING 99 OR 100 COMPL
013A 37        STC              )INDICATE NO BORROW
013B 73        MOV      A,B
013C CE00      ACI      0        )SETUP FOR 99 OR 100 COMP
013E 96        SUB      M        )99 OR 100 COMP OF PAT
013F EB        XCHG      )PAT ADR TO D,E-SUM ADR TO H,L
0140 86        ADD      M        )ADD SUM TO RESULT
0141 27        DAA              )BCD ADJUST RESULT
0142 EB        XCHG      )SUM ADR TO D,E-PAT ADR TO H,L
0143 12        STAX      D        )NEW LSB SUM BYTE
)**** NLSB SUBTRACTION
0144 13        INX      D        )ADR NLSB OF PAT
0145 23        INX      H        )ADR OF NLSB OF PAT
0146 73        MOV      A,B      )99H TO A
0147 CE00      ACI      0        )SETUP FOR 99 OR 100 COMPL
0149 96        SUB      M        )99 OR 100 COMP OF PAT
014A EB        XCHG      )PAT ADR TO D,E-SUM ADR TO H,L
014B 86        ADD      M        )ADD SUM TO RESULT
014C 27        DAA              )BCD ADJUST
014D EB        XCHG      )SUM ADR TO D,E-PAT TO H,L
014E 12        STAX      D        )NEW NLSB OF SUM
)**** NNLSB SUBTRACTION
014F 13        INX      D        )ADR OF NNLSB OF SUM
0150 23        INX      H        )ADR OF NNLSB OF PAT
0151 78        MOV      A,B      )LOAD A WITH 99H
0152 CE00      ACI      0
0154 96        SUB      M        )99 OR 100 COMP OF PAT
0155 EB        XCHG      )PAT ADR TO D,E-SUM ADR TO H,L
0156 86        ADD      M        )ADD SUM BYTE
0157 27        DAA              )BCD ADJUST
0158 EB        XCHG      )SUM ADR TO D,E-PAT ADR TO H,L
0159 12        STAX      D        )NEW NNLSB OF SUM
)**** MMSB SUBTRACTION
015A 13        INX      D        )ADR OF SUM MMSB
015B 23        INX      H        )ADR OF PAT MMSB
015C 78        MOV      A,B      )LOAD A WITH 99H
015D CE00      ACI      0
015F 96        SUB      M        )99 OR 100 COMPL OF PAT
0160 EB        XCHG      )PAT ADR TO D,E-SUM ADR TO H,L
0161 86        ADD      M        )ADD SUM MMSB TO RESULT
0162 27        DAA              )BCD ADJUST
0163 EB        XCHG      )SUM ADR TO D,E-PAT ADR TO H,L
0164 12        STAX      D        )NEW MMSB OF SUM

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MSB SUBTRACTION
0165 13      INX      D      ;ADR MSB OF SUM
0166 23      INX      H      ;ADR MSB OF PAT
0167 78      MOV      A,B    ;LOAD A WITH 99H
0168 CE00    ACI      0      ;
016A 91      SUB      C      ;PAT MSB WITHOUT SIGN SAVED IN C
016B EB      XCHG     H,L    ;PAT ADR TO D,E-SUM ADR TO H,L
016C 86      ADD      M      ;ADD IN SUM BYTE
016D 27      DAA       ;BCD ADJUST
016E EB      XCHG     H,L    ;SUM ADR TO D,E-PAT ADR TO H,L
016F 12      STAX     D      ;NEW MSB OF SUM

;
;**** UPDATE CURRENT EVENT CLOCK WITH CYCLE VALUE
;
0170 2A5E00  STEP5:  LHLD   SAV      ;PUT ADR OF START THIS EFFECT IN
0173 55      MOV      D,L      ;SAVE LOW ADR IN D
0174 7D      MOV      A,L      ;
0175 C60A    ADI      10      ;ADDING 8 GETS ADR OF CYCLE RATE
0177 6F      MOV      L,A      ;POINT H,L AT CYCLE RATE
0178 4E      MOV      C,M      ;LOAD LSB OF CYCLE RATE
0179 2C      INR      L        ;ADR OF MSB OF CYCLE RATE
017A 46      MOV      B,M      ;LOAD B WITH MSB OF CYCLE RATE
017B 6A      MOV      L,D      ;POINT H,L AT CURRENT EVENT CLOCK
017C 5E      MOV      E,M      ;LOAD LSB OF CUR EVENT
017D 2C      INR      L        ;ADR OF NMSB OF CUR CLOCK
017E 56      MOV      D,M      ;LOAD NMSB OF CUR EVENT CLOCK
017F 2C      INR      L        ;ADR OF MSB OF CUR EVENT
0180 AF      XRA      A        ;ZERO A
01C1 EB      XCHG     H,L      ;ADR TO D,E-LSB,NMSB OF CUR EV TO
0182 09      DAD      B        ;UPDATE LSB AND NMSB OF CUR EVENT
0183 EB      XCHG     H,L      ;ADR MSB TO H,L-VAL TO D,E
0184 0E      ADC      M        ;ADD C+MSB CUR EVENT+CARRY
0185 77      MOV      M,A      ;UPDATE MSB OF CUR EVENT CLOCK
0186 2D      DCR      L        ;ADR NMSB OF CUR EVENT
0187 72      MOV      M,D      ;UPDATE NMSB CUR EVENT
0188 2D      DCR      L        ;ADR OF LSB
0189 73      MOV      M,E      ;UPDATE LSB CUR EVENT CLOCK
018A 47      MOV      B,A      ;SAVE MSB CUR EVENT
018B 4D      MOV      C,L      ;SAVE ADR LSB CUR EVENT

;
;**** COMPARE STOP CLOCK WITH CURRENT EVENT CLOCK-IF TI
;**** TO END THIS EFFECT SET CURRENT EVENT CLOCK TO MAX
;
018C 3E0E    MVI      A,14     ;OFFSET TO EFFECT STOP
018E 85      ADD      L        ;L HAS START THIS EFFECT
018F 6F      MOV      L,A      ;POINT H,L AT EFFECT STOPMSB
0190 78      MOV      A,B      ;MSB CUR CLOCK SAVED IN B
0191 DE      CMP      M        ;COMPARE MSB CUR TO STOP
0192 C29E01  JNZ      CLC      ;
0195 7D      MOV      A,E      ;E HAS NMSB OF CUR EVENT
0196 2D      DCR      L        ;ADR NMSB OF STOP CLOCK
0197 DE      CMP      H        ;COMPARE NMSB CUR TO STOP
0198 C29E01  JNZ      CLC      ;
019B 7D      MOV      A,E      ;LOAD LSB CUR EVENT CLOCK
019C 2D      DCR      L        ;ADR LSB OF STOP CLOCK
019D DE      CMP      H        ;COMPARE LSB OF CUR TO STOP
019E D29E01  JNC      CLC      ;NO CARRY SET, CAN'T STOP

```

```

;
;**** SET CUR EVENT CLOCK FOR THIS EFFECT TO MAX
01A1 69      MOV      L,C      ;ADR LSB CUR EVENT CLOCK TO L
01A2 3EFF    MVI      A,0FFH
01A4 77      MOV      M,A      ;MAX LSB BYTE
01A5 2C      INR      L        ;ADR INSB CUR EVENT
01A6 77      MOV      M,A      ;MAX INSB
01A7 2C      INR      L        ;ADR MSB OF CUR EVENT
01A8 77      MOV      M,A      ;MAX MSB
;
;**** CHECK FOR MORE EFFECTS
;
01A9 3A5E00  OK:      LDA      5EH      ;LOAD LOW BYTE OF START ADR THIS
01AC C60F    ADI      15      ;GET ADR OF START NEXT EFFECT
01AE F65D    CPI      5DH      ;5DH IS OUT OF EFFECT TABLE
01B0 6F      MOV      L,A
01B1 C27300  JNZ      STEP1      ;NOT EQUAL TO 5DH THAN HAVE ANOTH
;
;**** HAVE CONSIDERED ALL THREE EFFECTS-CONVERT VALUE I
;**** TO BINARY TWO BYTE FORM OF INTELL
;
01B4 112800  LXI      D,5FREQ      ;ADR OF LSB OF SUM
01B7 1A      LDAX     D      ;LOAD LSB OF SUM
01B8 2603    MVI      H,TEN      ;ADR OF TEN/UNIT CONVERSION TAB
01BA 6F      MOV      L,A      ;VAL OF MILL 10/UNIT VAL IS INDEX
01BB 4E      MOV      C,M      ;SAVE BIN EQUIV OF MILL 10/UNITS
01BD 1C      INR      E      ;ADR OF HLB OF SUM
01BD 1A      LDAX     D      ;LOAD HERTZ UNIT/MILLI 100 BYTE
01BE 47      MOV      B,A      ;SAVE HLSB
01BF E60F    ANI      0FH      ;MASK OFF HERTZ UNITS VAL
01C1 07      RLC      ;DOUBLE 100 VAL TO GET TAB OFFSET
01C2 C69A    ADI      154      ;ADD IN BASE OF 100 BIN TABLE
01C4 6F      MOV      L,A      ;POINT H.L AT 100 BIN EQUIV
01C5 5E      MOV      E,M      ;LOAD LOW BYTE OF MILL 100 BIN EQ
01C6 23      INX      H
01C7 56      MOV      D,M      ;HIGH VAL OF MILLI 100 BIN EQUIV
01C8 69      MOV      L,C      ;LOAD MILLI 10/UNITS VAL
01C9 2600    MVI      H,0
01CB 19      DAD      D      ;MILLI BIN EQUIV IN H,L
;**** MILLIHertz OUTPUT
;
01CC 7C      MOV      A,H      ;HIGH BYTE VAL
01CD 2F      CMA
01CE D309    OUT      9      ;OUTPUT HIGH BYTE VAL
01D0 7D      MOV      A,L      ;LOAD LOW BYTE VAL
01D1 2F      CMA
01D2 D308    OUT      8      ;OUTPUT LOW BYTE VAL

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\*\*\*\*\* HERTZ CONVERSION

```

;
01D4 78      MOV      A,B      ;INLSB OF SUM SAVED IN B
01D5 1F      RAR              ;SHIFT HIGH 4 BITS TO LOW 4 BITS
01D6 1F      RAR
01D7 1F      RAR
01D8 1F      RAR
01D9 E60F    ANI      0FH      ;MASK OUT HIGH 4 BITS
01DB 4F      MOV      C,A      ;SAVE HERTZ UNITS VAL
01DC 112A00  LXI      D,SFREQ+2 ;ADR OF HERTZ 100/10 BYTE
01DF 1A      LDAX      D        ;LOAD HERTZ BCD 100/10 BYTE
01E0 6F      MOV      L,A
01E1 2600    MVI      H,0
01E3 29      DAD      H        ;DOUBLE 100/10 VAL TO GET BIN TAB
01E4 110004  LXI      D,C400H   ;ADR OF 100/10 BIN EQUIV TABLE
01E7 19      DAD      D        ;ACTUAL ADR OF HERTZ 100/10 BIN V
01E8 5E      MOV      E,M      ;LOAD LOW BIN EQUIV
01E9 23      INX      H        ;ADR OF HIGH BIN EQUIV
01EA 56      MOV      D,M      ;LOAD HIGH BINARY EQUIV
01EB 69      MOV      L,C      ;LOAD HERTZ UNITS
01EC 2600    MVI      H,0
01EE 19      DAD      D        ;HERTZ BIN EQUIV IN H,L

```

\*\*\*\*\* HERTZ OUTPUT

```

;
01EF 7C      MOV      A,H      ;HIGH BYTE VAL
01F0 2F      CMA
01F1 D30B    OUT      11      ;OUTPUT HIGH BYTE VAL
01F3 7D      MOV      A,L      ;LOW BYTE VAL
01F4 2F      CMA
01F5 D30A    OUT      10      ;OUTPUT LOW BYTE VAL

```

\*\*\*\*\* KILLIHERTZ CONVERSION

```

;
01F7 112B00  LXI      D,SFREQ+3 ;ADR OF NMSB OF SUM
01FA 1A      LDAX      D        ;LOAD KHERTZ 10/UNIT BCD BYTE
01FB 2603    MVI      H,TEN    ;ADR TEN/UNIT BIN EQUIV TABLE
01FD 6F      MOV      L,A      ;BCD 10/UNIT VAL IS TABLE INDEX
01FE 4E      MOV      C,M      ;SAVE BIN EQUIV IN C
01FF 1C      INR      E        ;ADR OF MSB OF SUM
0200 1A      LDAX      D        ;LOAD KHERTZ 100/MEGA BYTE
0201 47      MOV      B,A      ;SAVE FOR MEGA CONVERSION
0202 E60F    ANI      0FH      ;MASK OFF MEGA BITS
0204 07      RLC              ;DOUBLE TO GET 100 TAB INDEX
0205 C69A    ADI      154      ;ADD TABLE BASE
0207 6F      MOV      L,A
0208 5E      MOV      E,M      ;LOW BIN EQUIV OF KHERTZ 100
0209 23      INX      H
020A 56      MOV      D,M      ;HIGH BIN EQUIV
020B 69      MOV      L,C      ;LOAD 10/UNITS BIN EQUIV
020C 2600    MVI      H,0
020E 19      DAD      D        ;KHERTZ BIN EQUIV

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```

;**** KHERTZ OUTPUT
;
020F 7C      MOV      A,H
0210 2F      CMA
0211 D30D    OUT      13      ;OUTPUT HIGH BYTE VAL
0213 7D      MOV      A,L      ;LOAD LOW BYTE VAL
0214 2F      CMA
0215 D30C    OUT      12      ;OUTPUT LOW BYTE VAL
;**** MEGA HERTZ CONVERSION AND OUTPUT
;
0217 78      MOV      A,B      ;MEGA BYTE SAVED IN B
0218 1F      RAR          ;SHIFT TO LOW 4 BITS
0219 1F      RAR
021A 1F      RAR
021B 1F      RAR
021C E60F    ANI      0FH      ;MASK OFF HIGH 4 BITS
021E 2F      CMA
021F D30E    OUT      14      ;OUTPUT MEGA HERTZ
;**** SEND LOAD PULSE
;
0221 3EFF    MVI      A,0FFH    ;LOW PULSE VAL
0223 D30F    OUT      15
0225 3EFE    MVI      A,0FEH    ;HIGH PULSE VAL=BIN 1
0227 D30F    OUT      15
;
;**** UPDATE SIMULATION CLOCK
;
0229 212000  LXI      H,SIM      ;ADR OF SIMULATION CLOCK
022C 5E      MOV      E,M      ;LSB OF SIM CLOCK
022D 2C      INR      L        ;ADR OF NMSB
022E 56      MOV      D,M      ;LOAD NMSB
022F 2C      INR      L        ;ADR OF MSB
0230 AF      XRA      A        ;ZERO A
0231 EB      XCHG          ;ADR TO D,E-VAL TO H,L
0232 010100  LXI      B,1        ;PUT A 1 IN E,C PAIR
0235 09      DAD      B        ;BUMP SIM LSB AND NMSB
0236 EB      XCHG          ;ADR TO H,L-VAL TO D,E
0237 8E      ADC      M        ;SIM MSB+CARRY+ZERO
0238 77      MOV      M,A      ;UPDATE SIM MSB
0239 2D      DCR      L        ;ADR OF NMSB
023A 72      MOV      M,D      ;UPDATE NMSB OF SIM CLOCK
023B 2D      DCR      L        ;ADR OF LSB
023C 73      MOV      M,E      ;UPDATE SIM LSB

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```

      /
      /**** COMPARE SIM CLOCK WITH SIM STOP FOR END SIMULATIO
      /
023D 2E2F      MVI      L,STOP+2  /LOAD ADR OF STOP CLOCK
023F EE        CMP      M        /COMPARE MSB OF SIM CLOCK TO STOP
0240 C24C02    JNZ      CHSTP
0243 2D        DCR      L        /ADR OF NMSB OF STOP CLOCK
0244 7A        MOV      A,D      /LOAD NMSB OF SIM CLOCK
0245 BE        CMP      M        /COMPARE WITH NMSB OF STOP CLOCK
0246 C24C02    JNZ      CHSTP
0249 2D        DCR      L        /ADR LSB OF STOP CLOCK
024A 7B        MOV      A,E      /LOAD LSB OF SIM CLOCK
024B BE        CMP      M        /COMPARE WITH LSB STOP CLOCK
024C DA6000    CHSTP: JC      STEP0 /DO ANOTHER CYCLE
024F C30000    JMP      00H      /RETURN TO THE MONITOR

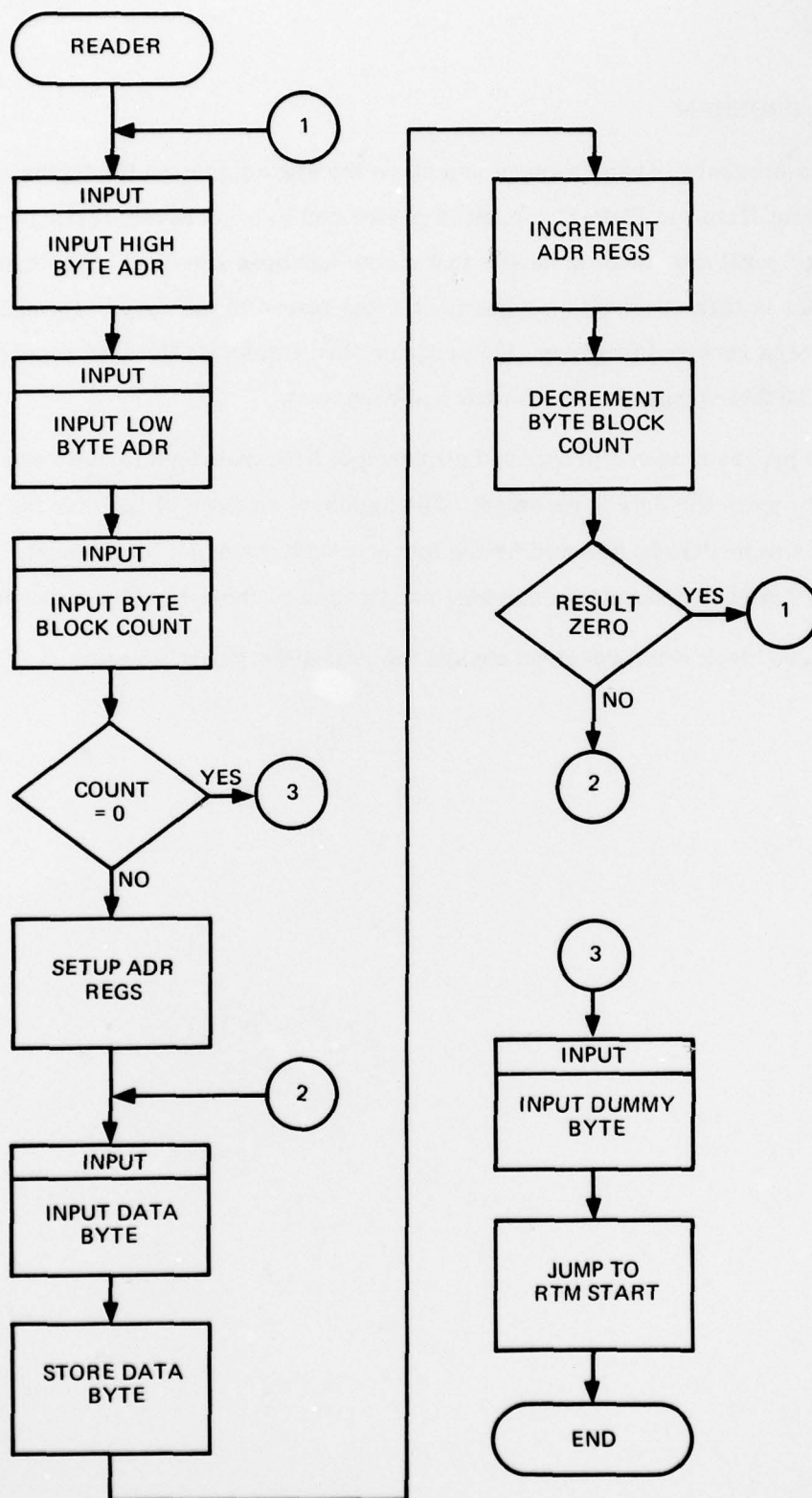
```

## READER PROGRAM

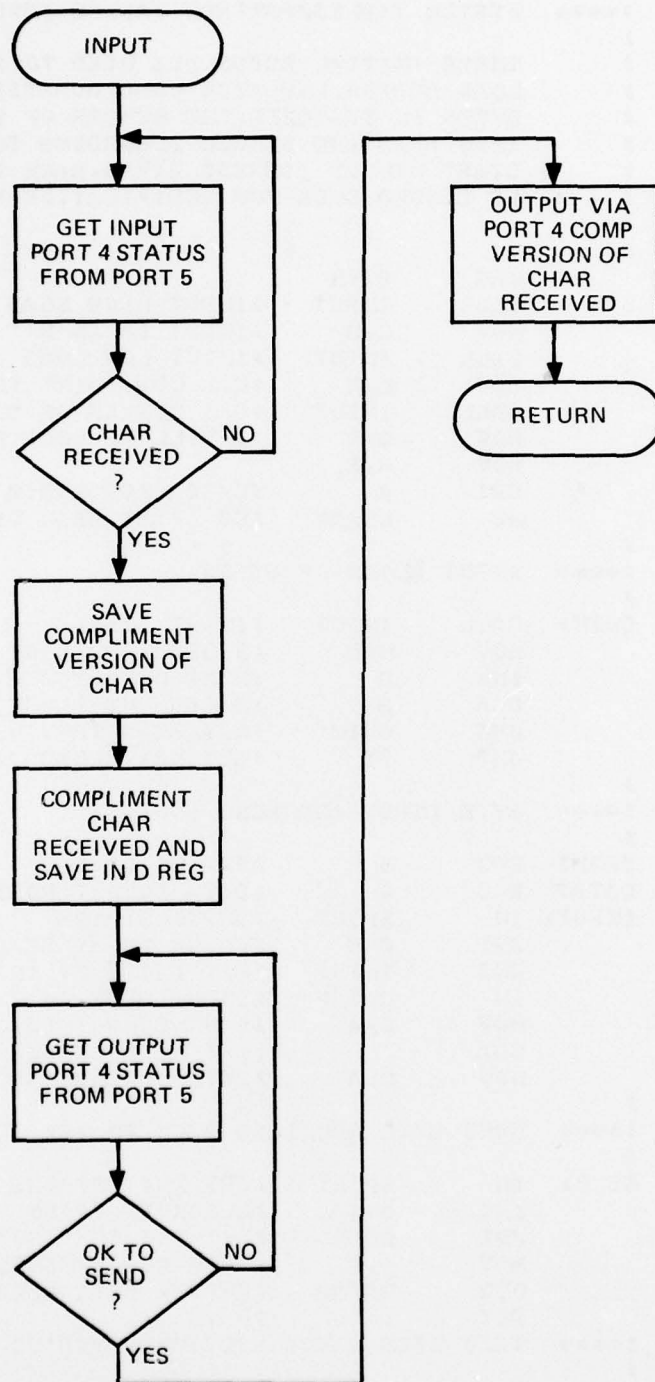
This program is used to input and store the system parameter tables and pattern tables output from the PDP-11. Input is performed by repetitively testing the status of input port 5 until the status indicates that a byte has been received. The byte sent from the PDP-11 is then received via input port 4 and stored in memory. To insure that the byte has been received properly, the program then transmits the byte received back to the PDP-11 that compares it with what had been sent.

The program uses a predefined sequence of byte transfers to determine where in memory to store the data it receives. The high byte address of the starting location is sent and is immediately followed by the low byte address and a block count. Data is then input and stored at consecutive memory locations until the byte block count is satisfied.

A zero block count received causes the real-time mode to begin.







```

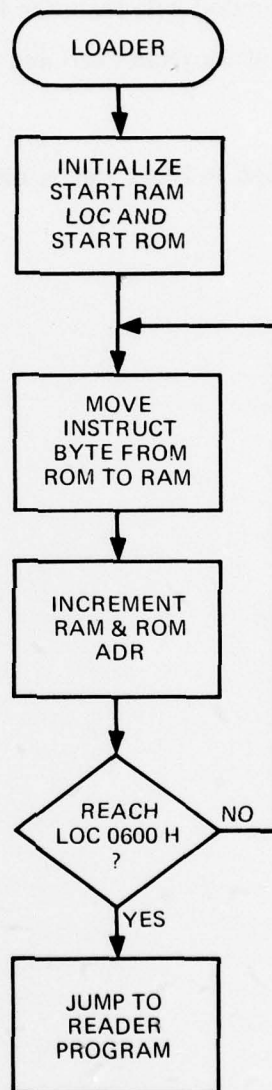
;
;
;**** SYSTEM TABLES/PATTERN TABLES INPUT ROUTINE
;
; THREE INITIAL READS ARE USED TO IDENTIFY HIGH BYT
; LOAD ADDRESS, LOW BYTE LOAD ADDRESS, AND NUMBER OF
; BYTES IN TRANSFER. THE NUMBER OF BYTES SPECIFIED A
; THEN READ AND STORED ACCORDING TO BYTE COUNT AND
; START MEMORY ADDRESS GIVEN. EACH BYTE READ FROM TH
; IS ECHOED BACK FOR VERIFICATION PURPOSES.
;
;
;
0252          ORG      270H
0270 CD8E02   ST:    CALL   INPUT    ;INPUT HIGH LOAD ADR
0273 62       MOV     H,D          ;INPUT IS IN D
0274 CD8E02   CALL   INPUT    ;INPUT LOW LOAD ADR
0277 6A       MOV     L,D          ;H,L NOW POINT TO START ADR FOR B
0273 CD8E02   CALL   INPUT    ;GET NUMBER OF BYTES IN BLOCK
027B 42       MOV     B,D          ;B WILL BE LOOP REG
027C 78       MOV     A,B
027D FE03     CPI      0          ;CHECK FOR END(0 BLOCK COUNT)
027F CAA502   JZ       LOADX      ;GO START REAL TIME PROGRAM
;
;**** INPUT BLOCK OF BYTES
;
;
0282 CD8E02   CHIN:   CALL   INPUT    ;INPUT BYTE
0285 72       MOV     M,D          ;STORE IN MEMORY
0286 23       INX      H          ;NEXT MEMORY ADR TO LOAD
0287 05       DCR      B          ;DECREMENT BLOCK COUNT
0288 C2C202   JNZ     CHIN        ;NOT ZERO THEN HAVE ANOTHER CHAR
028B C37002   JMP     ST          ;GET NEXT LOAD ADR, ETC
;
;**** BYTE INPUT AND ECHO ROUTINE
;
;
0285          SPORT   EQU      5      ;STATUS PORT
0286          DATAP   EQU      4      ;DATA IN/OUT PORT
028E DB05       INPUT:  IN       SPORT    ;INPUT STATUS
0290 EC01       ANI      01H          ;CHECK INPUT READY
0292 C28E02   JNZ     INPUT        ;BIT 0=1 THEN INPUT NOT THERE
0295 DB04       IN       DATAP        ;INPUT BYTE FROM THE 11
0297 4F       MOV     C,A          ;SAVE COMPLEMENTED VERSION
0298 2F       CMA          ;GET REAL VERSION OF INPUT BYTE
0299 57       MOV     D,A          ;BYTE IS RETURNED IN D
;
;**** ECHO BYTE RECEIVED BACK TO THE 11
;
;
029A DB05       ECHO:   IN       SPORT    ;GET WHIT STATUS
029C E604       ANI      04H          ;CHECK IF READY
029E C99A02   JNZ     ECHO         ;BIT 2=1 THEN NOT READY TO SEND
02A1 79       MOV     A,C          ;MOVE COMPLEMENTED VERSION
02A2 D304       OUT     DATAP        ;OUTPUT BYTE BACK TO 11
02A4 C9       RET
;
;**** ZERO BYTE COUNT RECEIVED-LOADING DONE-START RTN
;
;
02A5 CD8E02   LOADX:  CALL   INPUT    ;INPUT AND ECHO EVERY BYTE
02A8 C3C002   JMP     STEPS        ;START REAL TIME MODE
02AB          END

```

#### LOADER PROGRAM

This program is used to load the real-time program into RAM from its location in ROM. The program when executed will transfer the contents of locations 2C200 through 31FF to RAM beginning at location zero and cause program execution of the system tables, input routine.

This program is also located in ROM and is intended to act as a bootstrap loader of the real-time run.





```

;      KBAND REAL TIME PROGRAM LOADER
;
;      THE PURPOSE OF THIS PROGRAM IS TO MOVE THE KBAND
;      FROM ROM TO RAM AND INITIATE THE TABLE READ PART
;      THE PROGRAM.
;
;
0000      ORG      2B00H      ;ROM ADR FOR THIS PROGRAM
0270      RDR      EQU      270H      ;ADR OF TABLE INPUT ROUTINE
0000      RAM      EQU      0        ;START ADR IN RAM TO LOAD
2C00      ROM      EQU      2C00H     ;START ADR OF RTP IN ROM
;
2B00 110000      LXI      D, RAM      ;BEGIN ADR TO LOAD
2B03 21002C      LXI      H, ROM      ;ADR IN ROM TO BEGIN LOAD FROM
2B36 7E          INST:  MOV      A, M      ;LOAD A WITH INSTRUCT BYTE
2B07 12          STAX     D            ;MOVE INTO RAM
2B03 23          INX      H            ;NEXT ROM ADR
2B09 13          INX      D            ;NEXT RAM ADR
2B3A 7A          MOV      A, D        ;LOAD RAM HIGH ADR BYTE
2B0B FE06        CPI      06H        ;FINISHED LOAD AT 0600H
2B0D C2062B      JNZ      INST        ;JUMP TO TABLE LOAD ROUTINE
2B10 C37002      JMP      RDR
0000      END

```